4. Vertex Detector
The Vertex Tracker has to provide the jet flavor identification and accurate track reconstruction that are prerequisites to most if not all of the linear collider physics program. In some detector concepts, the vertex detector takes on an added role of charged particle pattern recognition as well. If the Higgs boson exists and is light, as the data collected so far indicate, its couplings to fermions of different flavour and mass must be accurately measured to test the Higgs mechanism of mass generation. Efficient flavor tagging in multi-jet events and determination of heavy quark charge will be instrumental to study signals of New Physics both through the direct production of new heavy particles, coupled predominantly to $b$ and $t$ quarks, and through precision measurements of electroweak processes at the highest energies. Physics requirements push the vertex tracker specifications to new levels. While much has been learned in two decades of R&D on Si detectors for the LHC experiments, the linear collider requirements motivate new and complementary directions for detector development. The linear collider environment, with its lower event rates and lower radiation, admits Si sensors that are substantially thinner, more precise and more segmented than at the LHC. Technologies which have not been applicable in the high radiation environment of proton colliders are available, as well as sensors based on new concepts. Significant R&D is required to solve the detector problems of the LC environment. CCD vertex detectors have already demonstrated very high resolution and segmentation with moderate multiple scattering. But for the CCD technology to be applicable to the LC improved radiation hardness and a factor of 100-1000 increase in readout speed are required. Technologies successfully developed for the LHC program, such as hybrid pixel sensors, are sufficiently radiation hard and can be read out rapidly. But they now need to be developed into much thinner devices with smaller cell size to improve their tracking resolution capabilities. Finally new technologies, such as CMOS sensors, have emerged as potentially attractive solutions. But they need to be demonstrated on large scales and be tailored to the linear collider application. These developments need to be guided by a continuing program of physics studies and detailed simulations to define the optimal designs and technology choices.

Contents

Overview and contents.........................................................................................................................134

4.1 Pixel Vertex Detector R&D for Future High Energy Linear e+ e- Colliders (Charlie Baltay: renewal) ..............................................................................................................137

4.2 Design of a Monolithic Pixel Detector Module (Marco Battaglia: renewal)........147

4.4 Vertex Detector Mechanical Structures (Henry Lubatti: renewal)................155

4.5 A Pixel-level Sampling CMOS Vertex Detector for the ILC (Gary Varner: renewal) .. .................................................................................................................................165

135
4.1: Pixel Vertex Detector R&D for Future High Energy Linear e+ e- Colliders

(renewal)

Vertex Detector

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Institution(s)
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Yale

FY07: 113,000
FY08: 125,000
Pixel Vertex Detector R&D for
Future High Energy Linear $e^+e^-$ Colliders

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University of Oregon

C. Baltay, W. Emmet, H. Neal, D. Rabinowitz
Yale University

Over the past two years of this R&D project, in collaboration with SARNOFF, Inc., we have developed a conceptual design for a Monolithic CMOS Pixel detector that we believe will satisfy the requirements of the Vertex Detector for the ILC, and that SARNOFF believes they can build. This design has been described in detail in our recent proposals as well as reports at recent conferences (D. Strom at Snowmass 2005, J. Brau at Bangalore LCWS 2006, C. Baltay at SLAC-Novosibirsk Instrumentation Conference, April, 2006, and J. Brau at the Hiroshima Semiconductor Detector Conference, Carmel, September, 2006). A detailed description of this design is in the report titled “HEP Vertex Detector Macropixel Design” by Saroff Corporation, dated February 28, 2006 is appended to the supplemental proposal submitted earlier in 2006 (http://www.hep.uic.edu/LCRD/FY07-08_detector_supplements/LittleBigDoc_numbered.pdf).

The currently approved FY 2006 funding for this project will allow SARNOFF to carry out the detailed design of the first prototype devices, resulting in a “tape out” from which the prototypes can be fabricated. The current estimate is that this will be completed by December of 2006. The present plan is to use the FY 07 supplement that we requested (but that has not yet been a proved by the DOE) to start the actual fabrication of the first set of prototypes. The FY 07 funding requested in this proposal would be used to complete the first prototypes and get started on the second set of prototypes. The FY 08 funding we plan to request when the time comes is expected to finish the fabrication and carry out the testing of the second prototypes, as detailed in the budget plan at the end of this proposal.

1. Introduction

Studies carried out in the U.S., Europe, and Asia, have demonstrated the power of a pixel vertex detector in physics investigations at a future high energy linear collider. At one time, silicon CCD’s (Charged Coupled Devices) seemed like the detector elements of choice for vertex detectors for future Linear $e^+e^-$ Colliders. However, with the decision for a cold TESLA-like superconducting technology for the future International Linear Collider (ILC), the usefulness of CCD’s for vertex detection has become problematical. The time structure of this cold technology is such that it necessitates an extremely fast readout of the vertex detector elements and thus CCD’s as we know them will not be useful. New CCD architectures are under development but have yet to achieve the required performance. For these reasons there is an increased importance on the development of Monolithic CMOS pixel detectors that allow extremely fast non sequential readout of only those pixels that have hits in them. This feature significantly decreases the readout time required. Last year, recognizing the potential of a Monolithic CMOS detector, we initiated an R&D effort to develop such devices. Another important feature of our present conceptual design for these CMOS detectors is the possibility of putting a time stamp on each hit with sufficient precision to assign each hit to a particular bunch crossing. This significantly reduces the effective backgrounds in that in the reconstruction of any particular event of interest we only need to consider those hits in the vertex detectors that come from the same bunch crossing.

2. Straw Man Vertex Detector Design

The overall vertex detector design we are working towards is shown in Figure 1, and the numbers and sizes of the 120 detector elements (chips) are summarized in Table 1.
The detailed time structure of the ILC is still to be settled on in the future. For the purposes of our present design we are using the time structure of the TESLA design, shown in Figure 2. We assume that the ILC design will have the same basic features. This design has 2820 bunches in a bunch train, with 5 bunch trains per second. The separation between bunches 337 nanosec, which makes each bunch train about 1 millisecond long, with about 200 millisecond between bunch trains.
Extensive background calculations\(^4\) indicate that the maximum total hit rate in the innermost layer of the vertex detector will be 0.03 hits/mm\(^2\)/bunch crossing.

Will use 12.5 cm x 2.0 cm as a typical chip size as an example, and for hit rates we will use the estimates for the innermost layer. Clearly the chips further out and the smaller chips in the forward disk layers will represent an easier problem.

3. Progress on Monolithic CMOS Pixel Detector Design

During the past two years a feasible conceptual design for a monolithic CMOS sensor that should meet the ILC vertex detector requirement has been developed in collaboration with SARNOFF (RCA’s silicon fabrication house) through an R&D contract. The report from Sarnoff of February, 2006 is attached to the supplemental proposal we submitted earlier in 2006 (http://www.hep.uiuc.edu/LCRD/FY07-08_detector_supplements/LittleBigDoc_numbered.pdf).

3.1 General Description of the Design

The current design is for chips up to 12.5 cm x 2.0 cm in size with a single layer of 10 \(\mu\)m x 10 \(\mu\)m pixels. Each pixel has its own electronics under it, but both the sensitive layer and the electronics are made of one piece of silicon (monolithic CMOS) which can be thinned to a total thickness of 50 to 100 \(\mu\)m, with no need for indium bump bonds. The electronics for each pixel will detect hits above an adjustable background. For each hit the time of the hit is stored in each pixel, up to a total of four different hit times per pixel, with sufficient precision to assign each hit to a particular beam crossing (thus the name “chronopixels” for this device). Hits will be accumulated for the 2820 beam crossing of a bunch train and the chip is read out during the 200 millisecond gap between bunch trains. There is sufficient intelligence in each pixel so that only pixels with one or more hits are read out, with the x,y coordinates and the time \(t\) for each hit. With 10 micron size pixels we do not need analog information to reach a 3 to 4 micron precision so at the present we plan on digital read out, considerably simplifying the read out electronics.

To get some feeling for the hit rates and occupancies we use the estimated 0.03 hits/mm\(^2\)/beam crossing for the worst case innermost layer. With 2500 mm\(^2\) per chip (a total of 25 x 10\(^6\) pixels/chip) and 2820 beam crossings per train we expect 2 x 10\(^5\) hits/chip/bunch train, or an occupancy of the order of one percent.

This appears much too high to allow efficient pattern recognition. The crucial element of our design is the availability of the time information (i.e., bunch crossing number) with each hit. If we trigger on an event that we are interested in from another part of the detector (tracker or calorimeter) with a time, i.e., the bunch crossing number known, we need to look only at those vertex detector hits which are consistent in time with

\[\text{Figure 2}\]
the event of interest and the occupancy drops to below $10^{-5}$ per pixel (SLD worked well with an occupancy of $\sim 10^{-3}$ per pixel in the Vertex Detector).

### 3.2 Detailed Design

SARNOFF has carried out a design of the electronics under each pixel of this chronopixel array. A schematic is shown in Figure 3 and a block diagram is shown in Figure 4. The functionality of this design has been verified by an hspice simulation.

---

**Chronopixel Array Architecture**

- As a local digital memory to store the time stamp, F/F's are used. To express 3000 bunches, 12 bits are needed and 13th and 14th bits are for checking the parity. Since average multiple impact probability per pixel is assumed to be 4, 14 (H) x 4 (V) F/F's are needed in this architecture.
- When a particle impacts, a pixel’s signal rises above the threshold level and comparator output switches from '1' to '0', enabling the F/F's to latch the time stamp data supplied by the global bunch counter. When the data is latched, the pixel is reset.
- If next particle impacts the same location, comparator output enables next set of F/F's to preserve the previous time stamp data. This is implemented using a counter which increments the row address of the F/F array.
- Time stamp information is read out in the random access mode from the pixels of interest which stored nonzero time stamp data.

---

Figure 3
The power consumption of this circuitry has been estimated. The analog parts of the circuit (the boxes labeled “Detector” and “Comparator” on Figure 3) consume most of the power, estimated at this stage of the design to be ~ 15 milliwatts/mm². The remaining digital components are estimated to be around 0.05 milliwatts/mm². The analog components are only needed during the time when hits are accumulated during the bunch train, ~ 1 millisecond. The average power can thus be reduced by a factor of ~ 100 by turning off the analog parts during the 200 millisecond digital readout. This would reduce the average power consumption to the vicinity of 0.5 watts per chip or to the order of 100 watts for the vertex detector, which seems acceptable.

### 3.3 Read Out Scheme

Each chip will consist of 2000 columns with 12500 pixels each. Each chip will be divided into 40 read out regions of 50 columns each. At the end of the bunch train when the electromagnetic interference due to the beam has died off the 40 read out regions will be read out in parallel at 25 MHz into a FIFO buffer located at the end of each chip. The contents of the FIFO buffer will be read out off the chip at 1 GHz. We thus expect to read out the full chip (2 x 10^3 hits, with 38 bits per hit) in about 8 milliseconds. This leaves a safety margin of 25 with the 200 millisecond gap between trains.
3.4 Fabrication Strategy

The expected read noise of about 25 electrons, and the demand for high efficiency with low backgrounds, sets the requirement for signal. Monte Carlo calculations indicate a 15 micron thick charge sensitive epitaxial layer will yield the required response of 800 electrons for a minimum ionizing particle crossing at normal incidence. Fabrication of chronopixel detectors on a 15 micron thick resistivity epitaxial layer will require the use of a custom CMOS process. We will produce our first prototype detectors using a standard process CMOS process that contains a 7 micron epitaxial layer with somewhat lower resistivity than will allow full depletion of the detector. This will allow the pixel electronic circuit to be tested at a reasonable cost, but the pixel will not be sensitive to minimum ionizing particles over its entire area.

The sensitivity of the first prototype detectors will be measured using a calibrated infrared laser and with an Fe-55 source. We are developing a detailed simulation of the sensitive portion of the pixel to facilitate these comparisons. Once the first prototype detectors have been verified we move to a custom CMOS process that will allow us to use custom wafers with properties required for the sensitivity over the entire pixel.

3.5 Charge Spreading

In order to be able to use digital readout the charge spreading has to be kept well below the pixel size. This can be accomplished by fully depleting the charge sensitive epitaxial layer.

4 Presently funded work.

Under the present contact, using the recently awarded ILC R&D funds for FY 2006, SARNOFF is proceeding with the detailed design of the Chronopixel Monolithic CMOS devices, as described in the February 28, 2006 report from SARNOFF referred to above. The detailed statement of work is as follows:

1. Layout Environment Setup
   Before a layout work starts, it is required to set up the CAD environment according to a given process technology. This work includes installing the design kit and various technical files provided from the foundry.

2. Chronopixel Layout
   Based on the Chronopixel schematic design, each component of the pixel needs to be translated into layout. Then, they are assembled together to form a Chronopixel layout.

3. Chronopixel array schematic design (Schematic, Simulation)
   Chronopixel array detector will consist of pixel array and readout circuits. Readout circuits consist of row decoder, row driver, column decoder, signal multiplex circuit, bias reference circuit, global bunch counter, timing controller, i/o interface. For each of the components, spice simulation will verify their functions and electrical performances including the noise performance with the size of signals expected. When all of the components are completed and assembled together, top simulation that integrates entire CMOS circuits will be implemented to verify the overall operation of the chip.

4. Floor-plan Design (Layout)
   Based on the schematic design, each of the component’s physical size and will be estimated. In addition, physical position of each circuit block will be investigated for the optimum utilization of the available silicon space. This careful floor planning will expedite the physical layout design.

5. Pixel-array Layout Design
   Physical layouts for each circuit components need to be created based on the schematic design. Once layouts of each component are completed, they are assembled together to form the entire array chip.
6. **Design Verification**
When the layout is completed, careful and through verification such as DRC and LVS will follow. DRC stands for design rule verification and LVS represents layout versus schematic.

7. **Tape-out**
This work is needed, for example, to ask process related questions, to place an order, to follow up tape-out procedure, to get feedback from foundry, to fix any problems in submitting the design, etc.

8. **Meeting and Documentation**
Technical meeting at Sarnoff, Teleconference, Presentation, Report.

**Deliverable:** Final Report, Tape-out to the Foundry, selected by the customer

This effort is expected to be complete by the end of December of 2006. At that time we will be ready to build and test the first set of prototypes.

5. **Future work for which supplemental funding is requested.**

As described above by early 2007 we (i.e. SARNOFF) will be ready to start the fabrication of the first set of prototype devices. It will be important not to lose momentum and proceed with this next stage of the project as soon after the completion of the present phase as possible.

5.1 **First Year (FY 2007)**

a) Starting with the “tape out” from the present stage of the project, SARNOFF will supervise the fabrication of the first set of prototypes. This first set will consist of 40 devices 5 mm x 5 mm each, using a 0.18 \( \mu \) technology, with 50 \( \mu \times 50 \mu \) pixels. The ultimate devices we are aiming for, to be fabbed ~ 5 years (?) from now, call for chips 125 mm x 20 mm each with 10 \( \mu \times 10 \mu \) pixels using a 0.045 \( \mu \) technology (which is not available now but is projected to be available and a mature technology 5 years from now). However, the smaller prototype devices with larger pixels will have all of the functionality of the final devices and are thus a very important test of the concept and the design.

b) Packaging of the prototype devices

c) Basic functional design testing at SARNOFF, including testing board design and fabbing

d) Detailed specific design testing and radiation testing to be carried out at Yale and the University of Oregon.

SARNOFF’s estimate for parts a, b, and c above is $145,000.

| Subcontract to SARNOFF for a, b, c, above | $145,000 |
| Fabrication of 40 prototype devices | $70,000 |
| Packaging of the prototype devices | 5,000 |
| SARNOFF Functional device testing, Consulting with UO and Yale during their testing, And Project Management | 70,000 |
| Building of test fixtures, testing of prototypes at Oregon | 17,500 |
| at Yale | 17,500 |
5.2 Second Year (FY 2008)

We expect that after testing the first prototype we will move on to the second set of prototypes. The details of this second set are not clear at this time since the details will depend on the performance of the first set of prototypes. However, we expect that the cost of the second set of prototypes will be similar to the first set with two exceptions:

i. There will be some costs associated with doing whatever redesign is needed for the second set of prototypes to be an improvement over the first set.

ii. The costs at SARNOFF for testing will be reduced since they will not have to redesign and refabricate a large fraction of their testing equipment.

We thus anticipate the following funding requirement for FY 2007:

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<th>Subcontract to SARNOFF for</th>
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<td>Redesign</td>
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<tr>
<td>Fabrication of prototypes</td>
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<tr>
<td>Packaging of prototypes</td>
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<td>Functional design testing at SARNOFF, project management, etc.</td>
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<tr>
<td>at Yale</td>
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<tr>
<td>Total</td>
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</table>

5.3 Two Year Budget Plan

As discussed above we expect this two year R&D plan, which will result in the fabrication and testing of two sets of prototypes, to require a total funding of

| Year 1                       | $180,000 |
| Year 2                       | $183,000 |
| Total                       | $363,000 |

Our proposal plan to obtain this funding is as follows

| FY 07 Supplement (already proposed) | $125,000 |
| FY 07 Base (this proposal)         | $113,000 |
| FY 08 Supplement                  | $125,000 |
| Total                             | $363,000 |

the detailed budget plan is given in the following table.

Detailed Spending Plan

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<th>FY07 Suppl</th>
<th>FY07 Base</th>
<th>FY08 Suppl</th>
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4.2: Design of a Monolithic Pixel Detector Module

(renewal)

Vertex Detector

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Institution(s)
U.C. Berkeley
LBNL

FY07: 25,430
Design of a Monolithic Pixel Detector Module

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and Lawrence Berkeley National Laboratory, Berkeley CA 94720, USA

Collaborators
Devis Contarato, Leo Greiner, Derek Shuman
Lawrence Berkeley National Laboratory, Berkeley CA 94720, USA

Project Leader
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Report of the Project Activities (July 2006 - November 2006)
The project started shortly after notification of approval in May 2006. The first stage concentrated on the back-thinning a batch of CMOS pixel sensor chips (MIMOSA-V chips, 17\times18 \text{ mm}^2, 1 \text{ M pixels}, 0.55 \text{ mm native thickness}) below 50 \text{ \mu m}, thermal characterisation of the STAR ladder prototype and FEA analysis of composite ladders. The chip back-thinning was carried out by Aptek Industries, San Jose, CA. Aptek uses a proprietary hot wax formula for mounting wafers and die to stainless steel grinding plates. The use of wax as an adhesive offers greater flexibility for handling thinner parts as well as eliminating the effects of ESD damage. The back-thinning is performed by a wet grind process with a rust inhibitor for cooling the chips and keeping the grind wheel free of debris which could cause damage when thinning below 100 \text{ \mu m}. The process allows accurate thickness measurements in-situ. After grinding, a polish process is performed which minimises the stress from the backside of the device and allows to achieve thicknesses below 50 \text{ \mu m}. Yields are dependent on various factors related to the quality of the silicon, including where in the ingot the wafers are taken from. Front-side processing factors such as oxides or polyamides as well as doping of a wafer can cause stress in the silicon lattice and may result in failure in the silicon at ultra thin specifications. The batch included a functioning chip as well as three non-functioning chips, to be used for mechanical characterisation. They have been thinned down to 40 \text{ \mu m}. At this thickness, chipping of the sensor edges was observed and the process was stopped. Inspection under a microscope revealed that the edges of the chip have been damaged, but only outside the guard ring area, thus not affecting the electrical functionalities of the device. Subsequent detailed tests, showed that thinning a CMOS pixel sensor below 50 \text{ \mu m} affects neither the noise nor its response to minimum ionising particles (see Figure 1). Detailed simulation and reconstruction of charged particle tracks in hadronic jets, performed with the Geant-4-based Mokka program and dedicated custom code developed by our group within the C++ Marlin reconstruction framework, have been used to study the impact of the sensor thickness on the track extrapolation accuracy. The Vertex tracker consists of five layers of 100 \text{ \mu m} carbon
composite ladders with sensors of variable thickness, providing 2.5 $\mu$m single point resolution. Preliminary results show that, below approximately 50 $\mu$m, the multiple scattering distortions to particle tracks are dominated by the contributions of the ladder support and of the beam-pipe. Therefore we shall start by considering sensor thicknesses in the range 40 to 60 $\mu$m, which our back-thinning R&D has proved to be feasible, from for this study.

One 40 $\mu$m-thick and one 50 $\mu$m-thick chips have been measured at a high-precision optical metrology machine to determine their shape. Ultra-thin Si loses most of the mechanical properties of unthinned sensors. In particular, the chip warps very significantly. It has been measured that the resulting deviations from flatness of an unmounted 40 $\mu$m-thick chip exceeds 1 mm. The sensor thickness has also been measured over its entire surface, by placing the chip on a vacuum chuck, and found to be constant, within $\leq 5$ $\mu$m.

In parallel to the back-thinning activity, work started for a detailed FEA simulation of a vertex tracker ladder. The ladder consists of 50 $\mu$m-thick CMOS pixel sensors, each measuring 30×30 mm, dissipating power along a 5 mm thick strip located along both outer edges, where ADCs and data sparsification electronics could be located. It is assumed that the electronics dissipates in the range 0.1-1 mW per column and can be power cycled. The sensors are mounted on a carbon composite support structure mounted at both ends. The ladder length is 15 mm. FEA simulation is also performed for the prototype STAR ladder, which had been built at LBNL and is made of 50 $\mu$m-thick Mimosa sensors mounted on a carbon composite support. As part of this LCRD project the thermal properties of the STAR prototype have been characterised. A heating cable has been attached to the ladder, which has been mounted on a test bench equipped with capacitive probes to measure its distortions and vibrations and an IR camera to monitor its temperature. A laminar airflow of variable speed has been applied. These measurements have been used to determine the maximum heat dissipation which can be removed by airflow, the ladder vibrations induced by the airflow and to validate the FEA simulation. The data collected in November is currently being analysed. This study will represent the foundation of a first detailed design of a very low mass ladder to hold the ultra-thin chips and offer the required material budget and mechanical stability.
PROJECT DESCRIPTION

Design of a Monolithic Pixel Detector Module

Personnel and Institution(s) requesting funding
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and Lawrence Berkeley National Laboratory, Berkeley CA 94720, USA

Collaborators
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Lawrence Berkeley National Laboratory, Berkeley CA 94720, USA

Project Leader
Marco Battaglia
MBattaglia@lbl.gov
(510) 486-7029

Project Overview
This proposal concerns the continuation, in its second year, of the project titled Design of a Monolithic Pixel Detector Module. It addresses the conceptual and engineered design of a ladder for the Vertex Tracker with the required mechanical stability and system integration, while minimising the amount of material. The Vertex Tracker performance is critical for accomplishing the objectives of the ILC in understanding key issues of particle physics from the origin of mass to its relation to the Cosmo. Preliminary simulation studies have shown that a single point resolution better than 5 µm and a material budget not significantly in excess to 0.1% X₀ per layer are needed to fulfill this goal.

While a very significant effort is being deployed in developing Silicon pixel sensors which are much more precise, thinner and faster than those ever installed in a particle physics experiment, only a limited attention has been devoted to the design of a detector module stiff enough to guarantee the sensor accuracy in the detector reference frame and light and integrated enough to offer minimal disturbance to the passage of particles and provide electrical and thermal services. The ILC Si sensor R&D has now successfully progressed to the stage when the design of a realistic detector module is needed to guide further R&D towards the choice of an optimal pixel sensor for the Vertex Tracker. There are three main open issues to which the proposed program could answer. The first concerns the optimisation of the sensor thickness. Early experience on sensor backthinning, to which our group contributes, shows that the thinning of pixel chips down to 50 µm and below is feasible. CMOS pixel chips have been backthinned to 50 µm and to the epi-layer (∼20µm), DEPFET test diodes to 50 µm and CCDs to 20 µm. These first tests have been successful and a more systematic characterisation of yields and performances is currently in progress. Below about 100 µm of thickness, the problems offered by mechanical stability and, possibly also charge collection, are becoming quite increasingly important and it is essential to leverage the advantage of a reduced material budget from thinner sensors with the increased requirements on the chip support structure. The goal of 0.1% X₀/layer is ambitious. The VXD3 detector at SLD, the
most precise vertex detector installed at a collider experiment, achieved 0.41% $X_0$/layer. Several concepts based on thin sensors mounted on various supports (carbon-fiber composites, Si carbide foam, diamond-coated composite materials are among those considered), which would amount to about 0.1% $X_0$, have been proposed and some studies are being carried out at RAL in the UK. The proposed project will continue the design of a low-mass detector module, with a support structure based on carbon composites and vitreous carbon foam, produce a prototype, mounting thinned Si chips and perform a full characterisation of mechanical behaviour and stability, including temperature and humidity cycling. In a possible second phase, beyond FY08, working detectors could be installed and the ladder tested under operational conditions, including power cycling. Sensor technology and detector concept specifics will be considered and both CMOS and DEPFET pixel sensors could be tested.

The second issue concerns chip cooling requirements, which has significant implications both in terms of sensor technology and material budget. We have started the study of airflow cooling both in terms of heat extraction, under realistic conditions such as power cycling, and in terms of ladder stability. This study is assessing the power dissipation threshold beyond which active cooling of the modules is needed and the module stability under temperature change and airflow-induced vibrations.

Finally, the design of a detector module will need to address the issue of the routing of signal lines and services, which also contribute to the overall material budget of a detector layer.

The project will also investigate offline software alignment procedures. This will be carried out, based on the experience gained by the LBNL group with the alignment of the Babar vertex detector at PEP-II. In FY07, we propose to build a test facility to study the ladder cooling and alignment. The test setup will reproduce the geometry of a Vertex Tracker made of five concentric barrel layers with constant coverage in polar angle. Ladders will be made of aluminium, with the exception of the prototype ladder(s) under test and mounted on plexiglass or aluminium end-rings. The test setup will be installed on an optical table and instrumented with temperature sensors, capacitive probes to survey temperature and displacements and an IR camera. Heating wires will simulate the power dissipation of the pixel electronics and a laminar airflow of variable speed will be applied. Such setup will allow to study the collective effect of the complex multi-layered tracker structure on cooling in rather realistic conditions.

This program will significantly profit of synergies with activities of other groups at LBNL in the Physics, Nuclear Science and Engineering Divisions, channeling the know-how accumulated in major projects, from CDF and Babar and the concurrent ATLAS and STAR projects, to the ILC application, minimising the cost-to-benefit ratio. We plan to extensively consult the team of engineers and technicians in charge of the ATLAS pixel mechanics and with the LBNL composite material group.

At the same time, we are actively engaged in reaching out to partner groups, engaged in R&D for the ILC Vertex Tracker, to share the resources made available through this project to a wider community. We have established contacts with SLAC, Fermilab, Purdue University, Max Planck Institute, Munich (Germany), Rutherford Appleton Laboratory, Didcot (UK), IReS, Strasbourg (France) and INFN, Italy. Max Planck Institute and IReS share pixel structures for the ladder construction and characterization. We shall keep close links with the detector concept groups, in particular the SiD Vertex group and the LDC Vertex contacts as well as other US institutions interested in Vertex Tracker R&D, which will have access to the facilities and expertise being established at LBNL.
Broader Impact

The development and deployment of increasingly complex high granularity trackers in particle physics experiments has come at the expense of increased material in the tracking volume. At next generation detectors for the ILC, but also for the LHC upgrade, tracking granularity and channel counts will increase even further. Lower mass is crucial at the LHC due to the tenfold increase in track multiplicity as well as at the ILC to provide the required precision track reconstruction and minimize the deterioration of calorimetric measurements.

This project aims at developing highly integrated electrical-mechanical-thermal structures with particular emphasis on material reduction. Experience earned in this project will benefit other applications in HEP and beyond relying on low-mass, high-resolution detectors.

As the activity described in the present proposal is being carried out as a collaboration between Universities and a National Lab, the project will see the participation of students. One UC Berkeley Engineering undergraduate is contributing to the project and we are actively seeking engagement of more students from the Engineering departments on the Berkeley campus. We also plan to involve an additional GSR, working part-time on software alignment and funded independently from this proposal. The project is also be open to undergraduate students, within the framework of the Undergraduate Research and Apprentice Program (URAP) at UC Berkeley, which is already offering research opportunities in the ILC program and has already effectively enabled under-represented minorities and disabled students to connect to research. The educational impact from student contribution to cutting edge research and technology development reaches far beyond the academic world because a large fraction of these students will find employment in industry. We shall actively encourage women and students from minority-serving institutions to join this program.

Results of Prior Research

Results of the semester of the project activity are given in a separate report. In addition, LBNL is engaged since the beginning of FY05 in an R&D program on advanced Si pixel sensors for the ILC. A part of this project addressed the study of backthinning of CMOS pixel sensors. Results of the successfull campaign of tests and measurements have been presented to several conferences, including SNIC06 Symposium at Stanford, the 2006 “Hiroshima” Conference and the 2006 Joint DPF/JPS Meeting and are being published on Nucl. Instrum. and Meth. A. The know-how and samples obtained with the backthinning activity, offers an important synergy with this project. In addition, the STAR group at LBNL, which collaborates to this project, is developing a very ambitious Vertex detector, based on CMOS pixel sensors, similar to those being considered for the ILC, and respecting almost equally tight constraints in terms of material budget. In addition, the know-how of the LBNL ATLAS engineering group in the field of composite materials is available to our project and it has recently been agreed to integrate more the ATLAS upgrade, STAR and ILC activities at LBNL. Their partnership ensures that this project will continuously profit from experience of cutting-edge solutions for low mass mechanics for detector applications, tailoring it towards the ILC requirements.

Facilities, Equipment and Other Resources

LBNL is well equipped for the production of support structures using composite material and their mechanical characterisation. Further, there is a very significant know-how on light-weight structures for high precision detectors in collider experiments. Work for the CDF Run2b upgrade has demonstrated the viability of a highly integrated Si detector module,
including cooling, support and embedded electronic bus-work. Experience with the ATLAS Pixel detector, whose mechanical structure has been designed and built at LBNL and is presently being installed at CERN, and the STAR vertex detector, being designed at LBNL for the STAR upgrade at RHIC, offers an important opportunity to start the ILC specific R&D on the foundation of state-of-the-art design concepts.

The ILC Advanced Detectors R&D Lab of our group has an environmental chamber which will be used to characterise temperature cycling and humidity effects on prototype ladders. We can also perform power cycling of CMOS pixel sensors to study power dissipation and survey the temperature gradient of prototype ladders using a high resolution IR camera. We have access to a fully equipped characterisation facility to perform studies of cooling and mechanical stability with nitrogen and air flow. This is equipped with a laser holography system which will be used to measure in real time distortions in prototype structures with sub-micron resolution. This system is very useful for looking at thermal distortions and small scale bending over a large area. A capacitive probe system measures the position of reference points with sub-micron resolution and a bandpass of 1 KHz. This is above the resonant frequencies of any of the structures that we intend to construct allowing to study for displacements and vibration induced by the air cooling or any other driving forces.

Alignment studies and data analysis will be performed at NERSC using the computing and data storage resources awarded to the ILC project.

**FY2007 Project Activities and Deliverables**

In the second year of this project, the ladder design will be finalised and one ladder prototype will be produced, equipped with at least one working detector chip and Si dummies of equal size and thickness. This will be characterised on the proposed test facility. Its stability will be studied with collimated lasers and the performance in terms of material budget will be assessed on the new LBNL ALS 1.9 GeV $e^-$ beamline at the BTS which is now equipped with a beam telescope made of thin CMOS pixel sensors. Finally backthinning test of new retical-size sensors produced in AMS 0.35-OPTO technology will be performed while DEPFET thinned structures will be made available at no costs by MPI, Munich as part of an ongoing collaborative effort.

**Budget justification:** Lawrence Berkeley National Laboratory

The budget request covers the cost of engineering support, production of one prototype and the limited additional equipment needed to extend the capability of the ILC detector lab in the characterisation of ladder prototypes.

We request support for 0.2 FTE from the Engineering Division at LBNL, if this will be awarded, matching funding should be made available by the Physics and Engineering divisions to make 0.5 FTE available to this program. The engineer will work in close contact with the group working at the design of the STAR vertex detector upgrade and adapt that design to the ILC specifications based on experience at STAR and ATLAS. In addition, we request 1 month of a mechanical engineer machinist and mechanical shop recharges for prototype production. Finally, funding is requested for part of the costs for the ladder test setup and chip backthinning.

**Institution:** Lawrence Berkeley National Laboratory, Berkeley CA.
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4.4: Vertex Detector Mechanical Structures

(renewal)

Vertex Detector

Contact person
Henry Lubatti
lubatti@u.washington.edu
(206) 543-8964

Institution(s)
Fermilab
SLAC
Washington

FY07: 33,083
ILC Detector R&D Project
Vertex Detector Mechanical Structures
FY 2007 Request
December 15, 2006

Personnel and Institution Requesting Funding

Henry J. Lubatti, University of Washington
Colin Daly, University of Washington
Tianchi Zhao, University of Washington
Mark Tuttle, University of Washington
William Kuykendall, University of Washington

Collaborators

1. Fermi National Accelerator Laboratory (Fermilab)
   William Cooper
   Marcel Demarteau

2. Stanford Linear Accelerator Center (SLAC)
   Su Dong

Collaborating personnel will work on the project but are not requesting funding here.

Project Leader

Henry J. Lubatti
lubatti@u.washington.edu
(206) 543-8964

Project Overview

We are requesting funding to continue the work with the Fermilab Si-detector group (Bill Cooper, Marcel Demarteau, et. al.) on the design and analysis of mechanical support structures for an ILC Vertex Detector. The University of Washington ground consists of members of the Physics Department (H. Lubatti and T. Zhao) and Mechanical Engineering Department (C. Daly, M. Tuttle and W. Kuykendall).

During the past year, despite severe budget constraints, we have developed and evaluated designs for low mass carbon-fiber support structures. FEA analyses of the mechanical and thermal properties were carried out and some prototype lay-ups were made. This proposed budget requests support to continue this work at a somewhat increased level.
The design goals of the proposed 5-layer vertex detector are that the support structures hold and maintain the position of the sensors, both within a sensor and among the full array of sensors, to a reproducible precision of better than 5 µm from one cool-down to the next. At operating temperature, variations in sensor geometry should be negligible during any period of less than a month.

The work proposed will continue to be carried out in close collaboration with personnel at Fermilab (Bill Cooper and colleagues). The Fermilab Group is the lead group for the work proposed here. The UW team concentrates on those aspects related to their proven competence in finite element analysis and design and fabrication of advanced carbon fiber/epoxy structures.

**Broader Impact**

In addition to the impact this work will have on the development of a precise and effective vertex detector for the ILC, it has the potential for impacts that go beyond the ILC experiment. Development of new techniques for fabricating low Z compact vertex detectors will certainly have an impact on the broader field of collider physics, both for high and intermediate energy experiments. Developing new ways to assemble geometrically complex carbon fiber structures could have an impact, and be useful, to our engineering colleagues who are developing high performance carbon fiber structures. This work will also have an impact on undergraduate education because we plan to engage undergraduate physics and engineering majors in this work, both as independent research students and as hourly workers. We have a tradition of involving undergraduates in all of our research efforts and believe that this is our most effective way of having a broader impact that touches the greatest number of people.

**Facilities, Equipment and Other Resources**

Since 1990, the University of Washington group (a collaboration of the Physics and Mechanical Engineering Departments) has been involved in the design and fabrication of several particle detector subsystems. These have included the muon subsystems for the SDC detector at the SSC, the end cap muon subsystem for ATLAS at the LHC and the Run2b upgrade to the innermost two layers of the silicon detector system at D0. The latter was de-scoped to be just the addition of a new layer0 to the Run2a system and this device has been completed, installed in D0 and is now running successfully. All of the D0 work has involved the design, FEA analysis and fabrication of very lightweight, stiff and precise carbon fiber/epoxy structures. As a result, the UW group has developed a major core competence in this area. Another new major resource is the FAA Centre for Excellence for Advanced Materials in Transport Aircraft Structures that has been established at the University. The major thrust of this center is R&D on advanced composite structures.

The University of Washington Physics Department machine shop is one of the largest physics department machine shops in the United States. We have available four CNC mills, one of which has a travel of 72” x 32” x 32”. We also have two CNC lathes
(turning centers), a wire EDM machine, a die-sinker, five conventional lathes and five conventional mills, all with digital readout. In addition, we have clean-room facilities with temperature control available, a Brown and Sharp Coordinate Measurement System (resolution 4 µm) and a Smart Scope (magnification x250, resolution 1µm) for precision measurements. The machine shop is staffed with six experienced machinists and tool & die makers. The joint work with Mechanical Engineering gives us access to that Department’s composite materials laboratory, which has available for our use a hot press, curing oven, and abrasive water jet cutter. That laboratory also has a large universal tension/compression testing machine that will be used to study the mechanical behavior of candidate materials and structures. For example, we are able to measure the orthotropic properties of various carbon fiber lay-ups. We also have access to an autoclave, and a larger oven in the Department of Material Sciences, which we used for fabrication of the D0 silicon vertex detector layer0 installation tooling. We estimate, in this project, approximately 100 hours of machine shop time per year, with the Physics Department contributing two-thirds of the cost on a cost-share basis. We have high performance PC workstations with the required CAD/CAM (Unigraphics) and FEA (Ansys) software and personnel with long experience with these systems.

Publications from prior support


Design and FEA Studies

Results for FY2006

Working in close collaboration with the Fermilab group, in the first year we have produced initial designs for a very lightweight carbon fiber/epoxy (CF) composite support structure for layer1 of the proposed 5-layer vertex detector (Figure 1). Solid models in our CAD system were used to generate finite element models in Ansys (Figure 2). The deflection of the structure under both gravity (Figure 3), and thermal loads was then calculated. Based on results of the FEA we designed and fabricated some prototype structures that have been sent to Fermilab for evaluation. Various modifications were made to the initial design to study their effects on deflection. While it was easy to get the gravity deflections within the desired limits, it has proved more difficult to keep the thermal deflection within these limits. He thermal properties of these thin, 4-layer CF lay-ups are not well predicted using the standard tools used in industry and it became apparent that we need to do actual experiments with simple models that can also be well understood analytically. This work has been initiated.

Proposed Work for FY2007
In the second year, we will continue the studies on the thermal properties of the CF structure materials both experimentally and analytically. Working from this, we will then continue to refine the design of the CF structure for layer1 using FEA studies. This will lead to further prototypes that will be evaluated at Fermilab after the addition of dummy silicon sensors. The major problem is the difference in the thermal expansion coefficients of the CF and the silicon sensors. We will obtain much thinner silicon ($\leq 50 \, \mu m$) as it is clear that the 320 $\mu m$ that we have is too thick.

Figure 1. UnigraphicsCAD solid model of layer1.

Figure 2. Ansys FEA model of layer1.

Figure 3. Deflection of Structure with Gravity Load in X-direction.

The end membranes on layer1 are very stiff in the radial direction and have not been modeled in detail until we have a better idea of the cable access requirements and the features needed to connect each layer to the complete vertex detector. These features will
be added to both the CAD and FEA models. The FEA work will be extended to the other 4 layers by generating a parametric model in Ansys. This will allow generation of a model of any layer by just changing a few parameters. The FEA analyses will be compared with tests done at Fermilab on prototype structures.

**Fabrication of Prototype Structures in FY2006.**

Work began in June of 2006 to develop fabrication techniques for a carbon fiber support structure for layer 1 of the proposed 5-layer ILC vertex detector. The first step was to build a simple lay-up mandrel with arbitrary dimensions within the general scale and geometry of the detector. This mandrel was used to identify fabrication issues related to this particular design concept and to evolve a fabrication process. Once a fully developed prototype design became available, including 3D solid models (Fig. 4), two identical precision steel mandrels were CNC machined.

![Figure 4. 3D model of prototype layer1 support structure.](image)

The first mandrel was used for lay-up of prototype parts. After several fabrication iterations, the lay-up and finishing processes have been refined, and a first set of three useful prototype structures have been produced and shipped to Fermilab. The thin, fragile support structures are easily broken if mishandled; therefore it was necessary to provide a plastic support mandrel with each prototype. These support mandrels were cast from a rubber mold created from one of the precision steel mandrels. Support structures and mandrels are shown in Figure 5. Structures are 4-ply lay-ups with [0,90,90,0] fiber orientations with the 0° fibers running longitudinally. Overall length is 130mm.
The second steel mandrel was sent to Fermilab to be used as a precision support surface during the installation of sensors and end-support rings. In order to safely handle the thin silicon sensors a special vacuum chuck has been fabricated (Fig. 6). This chuck was designed to mount onto existing silicon placement tooling at Fermilab.

The work described above was completed in December of 2006. The steel mandrels and the vacuum chuck body were fabricated by the UW physics instrument shop. The balance of the work was done by a 0.20 FTE engineer. A summary of layer1 fabrication deliverables is presented in Table 1.
Table 1: Layer1 completed deliverables.

<table>
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<th>Item</th>
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<tr>
<td>Proof-of-concept mandrel (aluminum)</td>
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<td>Proof-of-concept structures (carbon fiber/epoxy)</td>
<td>6</td>
<td>August 2006</td>
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<td>3D model of layer1 support structure (Unigraphics NX4)</td>
<td>1</td>
<td>September 2006</td>
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<tr>
<td>3D model of prototype mandrel (Unigraphics NX4)</td>
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<tr>
<td>Prototype mandrels (steel, CNC machined)</td>
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<td>Flat panels (carbon fiber/epoxy; various fiber angles)</td>
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<td>October 2006</td>
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<td>3D model of vacuum chuck (Unigraphics NX4)</td>
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<tr>
<td>Support mandrel mold (silicone rubber)</td>
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<td>Support mandrels (cast polyurethane)</td>
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<td>November 2006</td>
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<td>Template for cutting material (aluminum, CNC waterjet)</td>
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<tr>
<td>Prototype structures (carbon fiber/epoxy)</td>
<td>3</td>
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<tr>
<td>Vacuum chuck (aluminum body, porous ceramic plate)</td>
<td>1</td>
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Proposed Work in FY2007

The delivered layer1 prototype support structures will be fitted with dummy silicon sensors. The assemblies will then be measured under a variety of mechanical and thermal loading conditions. Results from these tests will be used to validate and refine FEA models, and to guide the direction of future design iterations. Evolution of the layer1 design will require continued fabrication and testing of prototype structures, as well as the further refinement of fabrication and assembly techniques. Design and fabrication of new tooling and fixtures will also be necessary. The scope of the work may be expanded to include the layer2-5 support structures, as well as pixel disk support structures. A comprehensive 3D CAD model of the vertex detector will be developed and maintained. Proposed activities and deliverables for 2007 are listed below:

- Measurements of assembled structure deformations between room temperature and operating temperature.
- Design, analysis, and fabrication of the next generation(s) of layer1 carbon fiber support structures.
- Design and fabrication of the next generation(s) of layer1 mandrels and assembly tooling as appropriate.
- Design, analysis, and fabrication of the first generation of layer2 carbon fiber support structures.
- Design and fabrication of the first generation of layer2 mandrels and assembly tooling.
- Fabrication of molds and polyurethane handling mandrels as needed.
- Design, analysis, and fabrication of prototype end-support rings (all layers).
- Design, analysis, and fabrication of the first generation of pixel disk support structures.
- Comprehensive FEA model of the evolving detector.
- Comprehensive 3D CAD model of the evolving detector.
- Engineering drawings of all delivered parts and tooling.
Budget Justification: University of Washington

The proposed structure design will be done in close collaboration with Fermilab personnel and this will require travel by C. Daly, Senior Engineer, to several working meetings at Fermilab to develop the design and to ensure integration of the structure with other detector components such as silicon detector chips, cables etc. H. Lubatti and T. Zhao will cover their travel through the NSF base grant.

Materials and supplies include carbon fiber prepreg and related lay-up supplies. In the second year, we will need to renew software licenses for CAD and FEA systems, for which we receive University rates that are shared with several groups.

Hourly student labor and shop costs relate to construction of the prototypes listed above. The costs are based on D0 Si-detector fabrication experience.

Budget (two year)
Institution: University of Washington

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Fringe Benefits calculated at 11.1% for hourly and at 27.1% for professional staff
Indirect Cost of 55.5% applied to Sr. Engineer salary/fringe benefits and all travel
* Jr. Engineer @ .20 FTE
+ Prof Colin Daly and Prof Mark Tuttle will not receive support during initial two years
** Travel to Fermilab for Sr. Engineer (approx. 4 trips, incl. car, per diem, etc)
++ Includes hours for machine shop as follows:
  Year 1 - 100 hours @ $70/hour of which 65% of cost will be contributed by the Physics Dept.
  Year 2 - 150 hours @ $70/hour of which 65% of cost will be contributed by the Physics Dept.

**Budget Justification: Fermi National Accelerator Laboratory**

Collaborating institutions, Fermilab and SLAC, are not requesting funding from this source.
4.5: A Pixel-level Sampling CMOS Vertex Detector for the ILC

(renewal)

Vertex Detector

Contact person
Gary Varner
varner@phys.hawaii.edu
(808) 956-2987

Institution(s)
Hawaii
Tokyo (Japan)
INP Krakow (Poland)
KEK (Japan)
Nova Gorca Polytechnic (Slovenia)
Melbourne (Australia)
National Taiwan University (Taiwan)

FY07: 45,900
A Pixel-level Sampling CMOS Vertex Detector for the ILC
Status Report and Project Initiatives

Precision vertex reconstruction at the ILC requires a detector capable of exquisite spatial resolution while withstanding significant low momentum charged particle fluxes and modest radiation damage. Lessons can be learned from the development of an ultra-thin CMOS pixel detector device for the high-occupancy environment of a Super B-Factory. The Continuous Acquisition Pixel (CAP) detector is based upon a Monolithic Active Pixel Sensor (MAPS) style architecture fabricated in a commercially available process. The capacity of pixel-level signal processing makes the device ideal for a future International Linear Collider (ILC) vertex detector.

We propose to continue to evolve the CAP architecture and verify the suitability of either a MAPS or a SOI technology implementation for the ILC through fabrication and evaluation of further prototype devices.

Contents

I. Personnel and Institution Requesting Funding 1
II. Collaborators 1
III. Project Leader 2
IV. Project Overview 2
A. Continuous Acquisition Pixel [CAP] 2
B. Choice of Technology 2
C. The CAP Architecture 3
V. Status Report 4
A. CAP Version 1 4
B. CAP Version 2 (Pipelined) 6
C. Beam Test Results
   1. CAP Version 3 (full-scale) 6
D. Further Prototypes 9
E. ILC Prototype
   1. Optimizing CAP architecture 9
   2. T-943 at Fermilab 10
VI. Facilities, Equipment and Other Resources 10
A. Instrumentation Development Laboratory 10
B. Hawaii Faculty, Researchers and Students 10
VII. FY2007 Project Activities and Deliverables 11
VIII. Proposed Budget and Justification 12
IX. Broader Impact 12
X. Project Activities and Deliverables Beyond FY2007 12
References 14

I. PERSONNEL AND INSTITUTION REQUESTING FUNDING

Given the level of funding available, Principle Investigator Gary Varner plans to support partially engineers Martin (ASIC design and test) and Rosen (mechanical support and thermal issues), as well postdoc Jin for ILC-specific ASIC development and evaluation.

Department of Physics & Astronomy
University of Hawaii at Manoa.

II. COLLABORATORS

As an outgrowth of the development effort for a Belle Pixel Upgrade, the CAP collaboration is highly international, with the University of Hawaii the only institution requesting direct support from the LCDRD.

The Belle pixel group consists of physicists and engineers from the KEK laboratory and the University of Tokyo (Japan), the H. Niewoniczanski Institute of Nuclear Physics in Krakow (Poland), the University of Pittsburgh, the Nova Gorica Polytechnic Institute (Slovenia), the University of Melbourne (Australia) and National Taiwan University (Taiwan). A breakdown of task sharing and institutional leaders for the Belle pixel effort is provided in Table I.

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</table>

TABLE I: CAP Pixel Collaboration.
These institutional responsibilities are a logical continuation of current activities within the Silicon Vertex Detector group. The Krakow group has built the readout chain for the current and original SVD, with KEK providing mechanical, integration and infrastructure support. Melbourne built most of the production silicon ladders that have been used in Belle and will be available for production work once they have concluded their ATLAS endcap silicon assembly. Radiation and environmental monitoring will be performed by Nova Gorica Polytechnical. Hawaii will focus on detector design and ladder mechanical structure. The Tokyo and Taiwan groups will focus on pixel vertex detector testing, evaluation and simulation. All these groups have expressed interest in extending this effort toward an ILC vertex detector, to the list of which, Ray Yarema’s group at Fermilab has also joined this development effort.

III. PROJECT LEADER

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IV. PROJECT OVERVIEW

The development effort detailed below is targeted toward the exquisite position resolution and occupancy requirements of the innermost components of a vertex detector of an ILC detector. While many groups worldwide are working on this problem, no prototypes to date yet have the speed, low-power, low-mass and mass manufacture capability needed to address the physics requirements. We apply lessons learned from the very challenging background conditions of a next-generation B-Factor vertex detector, to the list of which, Ray Yarema’s group at Fermilab has also joined this development effort.

A. Continuous Acquisition Pixel [CAP]

The Continuous Acquisition Pixel project was initiated by Varner [5] to explore improving the rate handling capability and resolution of the innermost layers of vertex detector for Belle at higher luminosities [6, 7]. As the success of this project has been demonstrated, it has been widely suggested during public presentations that this technology could be well matched to an ILC vertex detector. Of note is the sampling flexibility and in-pixel processing allowed by the use of a high quality CMOS process. This is seen in Fig. 1, where readout can be tailored to beam structure and thus reducing power draw, an essential feature for making an ultra-thin detector work without adding significant mass for cooling.

We describe below this progress and results from testing to date.

B. Choice of Technology

Until recently, the state-of-the-art in precision vertexing with pixels has been defined by the success of the CCD-based SLD detector [9] and the hybrid (sensor and ASIC readout electronics – bump-bonded together) devices developed for the ATLAS [10] and CMS [11, 12] detectors. However, despite the utility of these two types of pixel detectors for their particle physics experiments, they are not well matched to an ILC detector. Such LHC-type hybrid pixel detectors are too thick and have poor transverse resolution in each plane, which degrades the vertexing performance below Super-B [7, 13] and ILC requirements. While CCDs have impressive performance, as of yet their radiation hardness is insufficient [14] and their readout times are too long, or equivalently occupancy too high.

In the last few years groups in Strasbourg [15], LBNL [16], Hawaii [3] and others [17] have reported promising initial results with prototypes of so-called Monolithic Active Pixel Sensors (MAPS), which are thin, radiation-hard monolithic pixel detectors based on CMOS technology. A comparison between the standard Double-Sided Strip Detectors employed in Belle and a MAPS detector is shown in Fig. 2.

In MAPS the silicon epitaxial layer upon which the KEKB accelerator [1] can now produce in excess of one million B meson pairs per day. Upgrade plans call for increasing this luminosity by a factor of 30-50, providing huge data samples of 3rd generation quark and lepton decays. Precise interrogation of SM predictions will be possible, if a clean operating environment can be maintained. Extrapolation of current occupancies and radiation damage to this higher luminosity mandates the switch to a more robust vertexing technology than double-sided silicon strips. Initial prototype device development indicates that the Continuous Acquisition Pixel (CAP) [2–4] is capable of meeting these requirements.
B Choice of Technology

2.8k bunches, ~1ms long

Pre-sample N

CDS pair

Pre-sample N+1

Post-sample N

Orbit

Pre-sample NCDS pair

500ns

10us

Pixel Reset

Abort Gaps

Super KEKB

FIG. 1: The CAP architecture allows optimization of the sampling functionality to be made based upon the collision environment. In both the Super B Factory and ILC cases, this optimization involves taking advantage of the machine bunch structure to minimize power consumption – a necessity for operating an ultra-thin silicon detector.

Current DSSD

Because of large Capacitance, need Thick DSSDs ~ MAPS can be VERY Thin

300μm

MAPS

Key Features:
- Thermal charge collection (no HV)
- Thin - reduced multiple-scattering, γ conversion, background γ target
- NO bump bonding – fine pitch possible (8000x geometrical reduction)
- Standard CMOS process - “System on Chip” possible

FIG. 2: A comparison of current silicon tracking technology with that proposed for the upgrade. In MAPS only the top ~ 10μm are used, so devices can be made very thin. Because of the large capacitances involved with the Double-Sided Strip Detectors, a thick detector must be used to provide a sufficiently large charge signal.

1. Radiation Hardness

2. Readout Speed

3. Full-sized Detector

4. Thin (50μm thick) Detector Construction

To address these fundamental issues, a systematic development program has been established by the proposer.

C. The CAP Architecture

The operating principle of the Continuous Acquisition Pixel (CAP) architecture is illustrated in Fig. 3. The fundamental unit is a 22.5μm square pixel cell with a 3-transistor readout circuit (shown at the upper left part of the figure). Ionization electrons diffuse onto the gate of transistor M2, which forms the collection electrode. Since the collected charges are small, they are not transferred directly to the readout bus, but rather the threshold shift of M2 is detected by a sense current applied via individual pixel addressing through transistor M3. Transistor M1 resets the electrode potential at the end of each readout cycle.

The inset diagram in the upper right shows a sampling cycle. Immediately after reset, a sample is taken. During the integration time, leakage current is collected, leading to an expected difference compared with a sample taken at the end of integration. The detection of a charge particle passage is made by observing a larger than expected shift, as seen as the dotted line. In its simplest form, this CAP cycle is repeated indefinitely at high rate.

In KEKB, the beam circulation time is 10 μs. Collisions occur for 9 μs and there is a 1 μs-long “abort” gap when no beam particles are present. In the simplest CAP variant, frame samples are integrated during the 9μs live time and read out during the 1μs abort gap. The data from the most recent two cycles are stored and transferred continuously, thus the designation “continuous acquisition.” Operation in this mode provides great robustness against background. Extrapolating current backgrounds, an oc-
The CAP Architecture

C

The CAP Architecture

4

ADC

Pixel Array: Column select – ganged row read

High-speed analog

Low power – only significant draw at readout edge

Pixel Array of pixels

FIG. 3: Illustration of the Continuous Acquisition Pixel (CAP) detector operating principle, with the fundamental sensing circuit at the upper left, sampling cycle at the upper right, and flow out of the chip at the bottom. Details are provided in the text.

cupancy of well below 1% is expected [19]. A 1% occupancy corresponds to

\[
\left( \frac{1}{9 \mu s} \right) (2k \text{ pix/mm}^2) \left( 0.01 \text{ hits/pix} \right) \approx 2M \text{ hits/mm}^2 \cdot \text{s} \quad (1)
\]

which corresponds to a severe 16 MHz single silicon strip hit rate.

V. STATUS REPORT

The results shown below have largely been supported by the US-Japan Foundation, with funds coordinated through KEK and Fermi National Accelerator Laboratory. Additional salary support for participation by members of the University of Hawaii High Energy Physics Group is provided through DOE base support.

A. CAP Version 1

In order to gain experience with the capabilities and limitations of the MAPS technology, a first generation device, designated CAP1, was developed by the Hawaii group as shown in Fig. 4.

Fabricated in the TSMC 0.35\textmu m CMOS process [18], it consists of an array of 132 by 48 pixels, each 22.5\textmu m \times 22.5\textmu m.

A critical feature is the use of Correlated Double Sampling (CDS) to remove the intrinsic channel dispersion, as well as noise/quantum uncertainty due to reset. This process is illustrated in Fig. 5, which shows data taken with a radioactive source and an 8 ms sampling time. First differences are formed between samples from just after and just before a beam cycle that has produced a trigger of interest. A channel-by-channel leakage current correction is then applied.

Here when the difference is taken between successive sample frames, some peaks can be seen. Some of these are due to "hot" channels, i.e. channels that are known to have high leakage current. Of these more than 6,000 pixels shown, the worst case leakage current is only 18\textmu A. These are removed in the second step, when the channel-by-channel leakage current subtraction is made. After this, the hit candidate is clearly visible. The 8ms integration time for the test arrangement shown in the figure is almost 1,000 times longer than we plan to use at KEKB, there the leakage current will be negligible.

Figure 6 is an example of an event where a high energy particle traverses a stack of four CAP pixel detectors.

CAP1 Readout and Radiation Hardness. A crucial feature of deep sub-micron CMOS is its resistance to radiation damage. This was the key to earlier work by Varner [20] with others that resulted in an improvement of the radiation hardness of the Belle silicon vertex detector readout electronics. In order to evaluate radiation hardness and readout speed, the CAP1 was mounted into a readout board as seen in Fig. 7.

This choice of form factor proved very versatile, as all power and control could be provided over a single set of standard unshielded ethernet cable. All signals in and out are completely differential, to reduce radiated emissions. Even with a long cable, single pixel noise values of 16\textmu V were observed.

A series of radiation tests were performed with this set-up and are plotted in Fig. 8. Here the leakage current is plotted versus radiation dose for vari-
Frame 1 - Frame 2 =
- Leakage current Correction

~fA leakage current (typ)
~18fA for hottest pixel shown

Hit candidate!

FIG. 5: Graphic illustration of the Correlated Double Sampling and leakage current subtraction steps used to cleanly identify hit candidates in the CAP pixel detector.

FIG. 6: Detected event where a high energy particle traverses four CAP pixels. Note that the detectors are slightly misaligned.

FIG. 7: Readout configuration for the CAP1 detector.

ous periods of annealing, where the zero irradiation and 200kRad points are highlighted in the inset figure, demonstrating the clear evolution and spread in leakage current of all 6336 pixels as a function of irradiation. The accelerated dose rates are conservative when compared with an example from the published literature [21], made in the same fabrication process, shown as data points for comparison. These points correspond to slow exposure rates that are more like those that will occur in actual operation. (Practical limits on access to radiation sources precluded following the methodology of Ref. [21], though it will be considered for a final detector design.)

Even if we take the worst-case numbers from our
measurements and extrapolate to the short (i.e., 9 µs) integration times planned for Super Belle, the impact of these leakage currents will be minimal. A larger concern is the possible reduction in the charge collection efficiency, a topic that is being actively pursued. Recent results indicate [22] no charge collection efficiency loss up to at least 1MRad of 1 MeV γ exposure, which is the relevant damage benchmark for a B-factory environment.

B. CAP Version 2 (Pipelined)

A limitation observed during the testing of CAP1 was the readout rate that was actually achievable. While the small die could be read at the necessary 100kHz (10µs) frame rate, scaling to a larger detector indicated problems. A solution to the problem is to place pipeline storage inside each pixel, to decouple the sampling rate from the triggered readout rate. Therefore, in CAP2 a small, 8-deep pipeline was placed inside each pixel, as seen in Fig. 9. Here, the TSMC 0.35µm process was used again.

On the left, the standard 3-pixel cell is augmented with an array of 8 selectable storage cells. The outputs are independently accessible, completely decoupling storage from reading operations. On the right is the actual pixel cell layout, with various mask layers of different colors, indicating complete utilization of the available pixel area.

C. Beam Test Results

In order to evaluate the performance of CAP1 and CAP2 beam tests were performed at KEK and Fermilab. The same basic setup was used in both cases and seen in Fig. 10. The two views on the right show the array of 4 pixels located on the beamline; at the top, a clear view showing the co-alignment of the detectors and the bottom indicating the small footprint and required cabling plant. In the lower left figure may be seen the compact PCI crate containing the Backend (B-board) readout controller and embedded CPU. This test assembly is compact and self-contained, which makes it easy to deploy for beam tests of opportunity.

Many results have been reported from these tests [2, 3]. These include measurements of charge spread, SNR and noise level. A spatial resolution of just under 11µm at KEK as seen in Fig. 11. At top left is the detector layout. At top right is shown a residual self-determination method that uses Layer 4 [L4] and L2 to project onto L3 and compare with the L3 independent determination. The resultant residual histograms in the two axes perpendicular to the test beam are shown at the bottom left.

These resolutions are consistent with GEANT simulations of the detector spacing and materials used, which indicates that multiple-scattering dominates over the intrinsic resolution for this detector configuration with the relatively low momentum π beam used.

1. CAP Version 3 (full-scale)

One of the lessons learned from CAP2 was that with only 4 metal routing layers, insufficient power distribution caused significant baseline stability problems. To address this and to provide additional storage within each pixel, a third generation of CAP detector, designated CAP3, was fabricated.
FIG. 10: Various photographs of the June 2004 beam test at the KEK PS π− beamline. This compact test set-up readily fits in two suitcases and all of the power and signal cables were provided over standard network cables.

FIG. 11: Detector layout and spatial resolution results from a beam test of the CAP1 detector.

In Fig. 12 is seen the schematic representation (left) and layout diagram (right). Fabrication was moved to the TSMC 0.25µm process allowing an increase in the number of routing layers to 5, which improves power distribution and allows for 10 storage cells (8 for CAP2) within each pixel.

a. A full-sized CAP Detector. The most recent (third) generation CAP detector (CAP3) is shown in Fig. 13. These devices permit exploration of all of the outstanding issues, including processing the sensors to reduce the thickness for evaluation of heat extraction and mechanical support of thinned devices.

Indeed, the CAP3 detector is large enough to be considered for the basic building block of a complete pixel vertex subdetector, as drawn in Fig. 14 and in the process of preliminary mechanical design studies, with a focus toward thermal issues.
C  Beam Test Results

- 928 x 128 pixels = 118,784
- >43% active without active edge processing
- 21 mm Active area
- 20.88 mm >93% active without active edge processing

FIG. 13: Illustration of the 3rd generation of Continuous Acquisition Pixel detector. This “full size” device consists of almost 119,000 pixels. On the left, scale is given by comparison to coins. On the right, a zoomed in view of the bonding pads, spliced together with the view from the far end of the array, to indicate the small dead space involved.

- 32 CAP3/ladder
- 6 ladders/L1 layer
- 23 Mpixels
- 20-30kBytes/event (after L3)
- Scaling to high L (5x10^35): 0.5-1% occupancy
- SVD2.0 Ladders

FIG. 14: Engineering 3D model of a CAP3 ladder configuration, consisting of 6 ladders, each of which have 4 CAP3 sensors axially by 8 sensors in width. Experience gained in support and heat conduction will be valuable in considering a larger ILC detector array.

b. Laser Scan Tests. A crucial element of making a functional pixel detector subsystem is the ability to broadcast the data with low noise and power from the detector. The space allocated for this, at the interface between the detector and accelerator, is extremely congested and careful planning and monolithic integration are required to make such a system viable. A compact readout-flow scheme is illustrated in Fig. 15. CDS pairs are broadcast from the CAP3 detector and are analog-differenced and multiplexed in the nearby pixel readout chip (PIXRO1) [6] onto a single, high-speed analog fiber link to the electronics hut. Operation at the speed required to make this work was found to be unachievable in CAP3 due to the settling time on the long readout lines across the chip. This is due to the large capacitance of the readout bus lines, a known but pernicious problem.

FIG. 15: Planned data flow from pixel detector to Belle Data Acquisition system. A key element in this chain is the PIXRO1 chip, which is common to an ILC readout scheme.

The basics of the CAP3 development are presented in Ref. [8]. A sample laser pulse is seen in Fig. 16.

FIG. 16: Sample laser shot recorded with the CAP3 detector.

Laser scans across the 120k pixel array in a single device may be viewed online:

http://www.phys.hawaii.edu/~bellepix/ResultsSetUp.htm

Evaluation of the storage cells has indicated that the are strong bias effects which will make the proposed low duty-cycle operation at the ILC a challenge. This should not be surprising. For even a modest surge current of 20µA per pixel, with more than 100k pixels, this represents more than 2 Amperes! Great care in the operational ramping, bypassing and power wiring will be needed to operate in this mode.
D. Further Prototypes

Based upon the lessons learned from CAP3, the details of which will be covered in a subsequent publication, two new prototypes have been designed and submitted for fabrication. The first, CAP4, has actually been fabricated, as may be seen in Fig. 17.

![Die photograph of the CAP4 detector, and evaluation platform for three design concepts as described in the text.](image1)

CAP4 is an attempt to address two of the problems that were not adequately addressed in CAP3. The first is the readout speed of the long analog lines, being weakly driven. One option is to provide a threshold-level scan (e.g. Wilkinson-type) encoding of the stored analog information. This is one of the three options prototyped. The second two prototypes consider the second problem encountered. Specifically the data flow in the case of a Super-Belle vertex detector. As these architectures are not relevant to an ILC vertex detector, no further mention of them shall be made.

Last year we had the opportunity to prototype in a new Silicon-On-Insulator process that is under development by OKI Semiconductor\[23\], the various Test Element Group die of which are seen in Fig. 18. Due to exploratory choices of guard-rings and back-bias protection, full depletion was not possible in this first prototype round. A subsequent fabrication round, which closed in December 2006, has been joined by a number of groups worldwide. The advantage of SOI is that it can be operated in full depletion, which eliminates the issue of small signal yield, which has been endemic to the standard MAPS detectors.

Results from this next round should be available by late spring 2007. It is worth emphasizing that the commercial interest in this process is two-fold: to reduce power consumption from parasitic substrate capacitance, as well as intrinsically high radiation resistance. Both are attractive for an ILC detector for performance reasons.

E. ILC Prototype

We propose to design, fabricate and test an evolutionary descendant of the CAP architecture tailored to the planned ILC operating environment.

While the operating environments in the inner detection layers at Super B and the International Linear Collider are different, the requirements on thickness, data volume, low-power consumption and the instantaneous occupancy are actually quite similar, as may be seen in Table II. In these comparisons integration time is dependent upon the reset and sampling times needed, which is in turn related to the machine bunch structure shown in Fig. 1. In both cases the electronics operation is optimized to reflect the machine structure available, as described below. For the ILC, there are two options listed for some parameters, with the first for technologies capable of storing samples within a bunch train (Column Parallel CCD (CPCCD) with storage or CAP) and the second with longer integration time (higher occupancy) corresponding to devices without in-pixel storage (standard CCD or DEPFET).

Of the comparisons listed, it is interesting to note that the data rate and radiation tolerance requirements are actually more severe for Super Belle than for the ILC [24]. That is, any detector capable of successful operation in the Super B environment is a viable option for the ILC vertex detector.

1. Optimizing CAP architecture

In the first phase, we plan to pursue an ILC-specific CAP design, designated LCAP1, optimized for the ILC beam structure. As the CAP architec-
ture is quite flexible, it can be tailored for the machine operational environments, as mentioned earlier in Fig. 1. The first generation will explore issues of maximum sample storage depth. A future generation will follow up with lessons learned, as well as exploring ultra low-power operation, a major concern for reducing support infrastructure.

Discussions have been ongoing [26] on possible joint collaborative efforts to make a variant of the CAP architecture that is tailored to the ILC requirements. These discussions have affirmed that a device suitable for a high-luminosity Belle could also serve as a functioning prototype for a future ILC vertex detector. Given the long and uncertain development time table for completion of the ILC detector, it makes sense to develop experience through the completion and commission of a working pixel vertex detector system under demanding operating conditions.

2. T-943 at Fermilab

Varner is spokesperson for the T-943 experiment at Fermilab, which has the charge of evaluating the ultimate resolution of high sensitivity, pipeline operation MAPS devices. Evaluation of the LCAP detector will be performed at the Meson Test Beam Facility [27], where it will be necessary to have very high energy, minimum ionizing particles (120GeV/c protons) to confirm that the single-point resolution meets the µm-level ILC requirement.

VI. FACILITIES, EQUIPMENT AND OTHER RESOURCES

Considerable expertise and engineering resources are available at the University of Hawaii and our activities are well supported. We have two full-time machinists available through the Department of Physics and Astronomy machine shop, as well as the support infrastructure described below.

A. Instrumentation Development Laboratory

The CAP progress demonstrated up to this point would have been impossible without the support of an entire engineering team at the University of Hawaii. With strong support from the High Energy Physics Group, the Instrumentation Development Laboratory [28] develops world-class instrumentation such as the CAP pixel.

Dedicated to the development and support of high-performance instrumentation for world-class research in High Energy and Particle Astrophysics, the ID Lab is available to the University of Hawaii research community at large.

As can be seen in Fig. 19, the lab serves as host to a diverse group, bringing together talent from throughout Asia, Europe and North America.

Electronics design support consists of workstations and software for the design of printed circuit boards, FPGA/CPLD firmware and ASICs. Assembly benches and prototyping facilities, with available and well-trained student technician support, are maintained. Test instrumentation in NIM, 6U/9U VME, CAMAC, FASTBUS, compact PCI and LabView/GPIB are available. Silicon pixel and custom detector development are facilitated by a Cascade motorized probe station, Agilent parametric analyzer, K&S wire-bonder, all located inside an assembly clean room. Three SMT assembly/inspection stations are complemented by a BGA rework station.

The ID-Lab provides expertise in IC and board design, as well as software and firmware. Lab chief engineer Kennedy is coordinating the pixel readout system design. Engineering doctoral fellow Martin will complete the PIXRO1 as her dissertation topic. A particularly valuable asset is mechanical engineer Rosen, who designed the current Belle beampipe and will lead the mechanical design of the pixel ladder structure.

Excellent laboratory space is provided by the University, with over 2000 square feet available to the ID Lab, as can be seen in Fig. 20.
TABLE II: Comparison of Super B-Factory and ILC pixel vertex detector operating conditions. For the ILC there are often two parameters listed with a slash between, referring to the possible choice between candidate technologies. As no single technology has demonstrated itself capable of meeting all of the design and environmental requirements, it is expected that this R&D effort should remain active for the next few years, with a decision to be made in 2010 at the earliest [25]. Evolution of the CAP technology to meet these requirements shows real promise.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>ILC</th>
<th>Super-B</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integration time</td>
<td>25µs/1ms</td>
<td>≤ 10µs</td>
<td>Belle (trigger dep.)</td>
</tr>
<tr>
<td>BX collision timing</td>
<td>300 (150) ns</td>
<td>2 ns</td>
<td></td>
</tr>
<tr>
<td># bunches/integ. time</td>
<td>75(150)/2.8k</td>
<td>1-5k</td>
<td>CPCCD or MAPS/DEPFET for ILC</td>
</tr>
<tr>
<td>Expected occupancy</td>
<td>~ 1%</td>
<td>~ 0.5 – 1%</td>
<td>Belle extrapolation (max.)</td>
</tr>
<tr>
<td># pixel channels (Million)</td>
<td>100’s to 1k</td>
<td>10-50</td>
<td>5 layers versus single</td>
</tr>
<tr>
<td>Duty cycle (high power)</td>
<td>few %</td>
<td>5-10%</td>
<td>within acceptance</td>
</tr>
<tr>
<td>Readout cycle</td>
<td>between trains</td>
<td>continuous</td>
<td></td>
</tr>
<tr>
<td>Pixel readout rate (raw)</td>
<td>500/10 Gpix/s</td>
<td>200-1000 Gpix/s</td>
<td>Belle 10kHz trigger</td>
</tr>
<tr>
<td>Radiation requirements</td>
<td>0.5kGy/yr</td>
<td>few 10kGy/yr</td>
<td>neutron dose not considered</td>
</tr>
</tbody>
</table>

FIG. 20: Pictures of the excellent laboratory space and equipment available for CAP pixel development.

B. Hawaii Faculty, Researchers and Students

Faculty members Browder and Varner are active participants in this project. Senior researcher Parker is a wealth of information on silicon fabrication and processing. The CAP pixel project has been the primary task of post-doc Barbero, and will be for his replacement. Recently hired post-doc Jin will continue to be more heavily involved. Student Uchida has participated in all beam tests, with student Sahoo to join and gain hardware experience.

Our current DOE grant supports all of these group members. Pending this award, new student Nishikawa will join the effort and start detailed studies of detector optimization.

a. Other Facilities In addition to the full-time machinists and shop mentioned, the university also provides computing support and access to a high-performance computer farm.

VII. FY2007 PROJECT ACTIVITIES AND DELIVERABLES

In the second year the target will be to develop a first generation of ILC-specific sampling architecture. Our current studies show that down to quite small storage cell capacitances, as shown in Fig. 21, the kTC noise looks manageable. The current design exercise is to explore the maximum packing density possible, to maximize the number of storage cells, which reduces the effective occupancy for a given integration period.

FIG. 21: Contribution to noise due to storage cell capacitance. For small storage cells, this term can become important though this can represent a very small storage element.

The first ASIC design is designated LCAP1 (Linear Collider CAP #1) and the development timescale is matched to a fiscal year. From experience with three generations of CAP detector, this
is a reasonable interval in which to perform the tasks outlined below:

1. design – 3 months
2. fabrication – 3 months
3. eval board – 2 months
4. firmware – 2 months
5. test/document 2 months

The deliverables are a set of fabricated die after 6 months, a functioning die on test board, available for radiation, noise, resolution and other testing within 10 months. Finally, a publication documenting results of these test round out the year development cycle.

VIII. PROPOSED BUDGET AND JUSTIFICATION

A summary of the proposed budget for FY2007 is given in Table III. The budget is broken out by salary, travel, equipment fabrication, stipend, material & supplies and miscellaneous costs (shipping, document).

TABLE III: Total budget for FY2007, all values in K$.

<table>
<thead>
<tr>
<th>Item</th>
<th>FY07</th>
</tr>
</thead>
<tbody>
<tr>
<td>Salaries &amp; fringe</td>
<td>$0.0</td>
</tr>
<tr>
<td>Travel</td>
<td>$2.0</td>
</tr>
<tr>
<td>Equipment fabrication</td>
<td>$34.4</td>
</tr>
<tr>
<td>Stipend</td>
<td>$7.9</td>
</tr>
<tr>
<td>Other direct costs</td>
<td>$1.0</td>
</tr>
<tr>
<td>Indirect costs</td>
<td>$0.6</td>
</tr>
<tr>
<td>TOTAL</td>
<td>$45.9</td>
</tr>
</tbody>
</table>

b. Operations. Engineering support is costed as part of the LCAP1 equipment breakdown in Table IV. Stipend support will cover ASIC design and evaluation work by Martin and all work will be completed in 2007.

c. Travel. Travel is requested for the proposer and other participants to perform the measurements of detector performance as part of a beam test experiment at the Fermilab MTBF facility.

d. Equipment. We describe here the major fabricated equipment costs, which are dominated by the ASIC fabrication costs.

Costs for the first ILC detector prototype are listed in Table IV. This prototype builds heavily on the systems developed above. Some electrical engineering design time is required for an improved portable data acquisition system and to establish the data link. Student labor costs are not included here. Budgeting is based upon completion of the task within FY2007.

TABLE IV: ILC CAP “LCAP1” prototype budget.

<table>
<thead>
<tr>
<th>Item</th>
<th>Est. Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCAP1 ASIC fabrication</td>
<td>$17K</td>
</tr>
<tr>
<td>Engineering (mechanical)</td>
<td>$2.5K</td>
</tr>
<tr>
<td>Engineering (electrical)</td>
<td>$7.5K</td>
</tr>
<tr>
<td>ICs, parts &amp; materials</td>
<td>$2K</td>
</tr>
<tr>
<td>Board fabrication</td>
<td>$2.5K</td>
</tr>
<tr>
<td>misc. cabling, housing</td>
<td>$1.5K</td>
</tr>
<tr>
<td>Test structure assembly</td>
<td>$1.4K</td>
</tr>
<tr>
<td>Estimated total:</td>
<td>$34.4K</td>
</tr>
</tbody>
</table>

Common to these tasks, additional non-recurring engineering costs support the design and printed-circuit board layout capacity of the Instrumentation Development Laboratory.

IX. BROADER IMPACT

As one of the founding mentors, Varner was instrumental in establishing the Quarknet program in Hawaii. Being separated from the US mainland and Asia by thousands of miles of open ocean, it is essential to expose high-school teachers and local, underserved students to the excitement of frontier physics though our local activities. Our annual Physics Open Houses are very well-attended and being able to involve and interest the community at large is crucial.

Public support for funding of the ILC in the long-haul depends upon educating the educators, the next generation of students, and the general public in the exciting discovery possibilities at the ILC, and the very interesting technical challenges (being addressed right in Hawaii!) to meet them. This type of hands-on hardware exposure for the young and inquisitive pupils is sorely needed as collaboration sizes have increased.

X. PROJECT ACTIVITIES AND DELIVERABLES BEYOND FY2007

At the conclusion of this last year of the current funding umbrella we expect to have feedback not just from the LCAP1 prototype, but also for subsequent generations of Super Belle CAP pixel detector,
both MAPS and SOI. In the latter cases the experience with handling very thin devices and operating at high speed and low power will be valuable in shaping the direction of the next generations of system-level demonstrator prototypes. In the CAPS lineage, this would be designated LCAP2 and the development cost would be expected to increase as a “full sized” device fabrication would be requested.

Costs for this LCAP2 detector prototype are tabulated in Table V. This prototype will be an evolution based upon lessons learned with the LCAP1 prototype. It is assumed that a deeper submicron process will be used, consistent with evolving industry trends. Student labor costs are again not included here. Budgeting is based upon completion of this task in FY2007.

<table>
<thead>
<tr>
<th>Item</th>
<th>Est. Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCAP2 ASIC fabrication</td>
<td>$67K</td>
</tr>
<tr>
<td>Engineering (mechanical)</td>
<td>$2K</td>
</tr>
<tr>
<td>Engineering (electrical)</td>
<td>$5K</td>
</tr>
<tr>
<td>ICs, parts &amp; materials</td>
<td>$2K</td>
</tr>
<tr>
<td>Board fabrication</td>
<td>$2.5K</td>
</tr>
<tr>
<td>misc. cabling, housing</td>
<td>$1.5K</td>
</tr>
<tr>
<td>Test structure machining</td>
<td>$1.2K</td>
</tr>
<tr>
<td>Estimated total:</td>
<td>$81.2K</td>
</tr>
</tbody>
</table>

At the present time since none of the technologies demonstrated to date solve all of the speed, sensitivity and power requirements, it is necessary to continue to evaluate new technologies, such as the SOI process mentioned above. Moreover, it should be expected that consolidation of the various efforts will happen. Success and failure of these efforts will dictate the form the subsequent evolution shall take.


[11] A number of groups are pursing MAPS-based detectors for the ILC. In addition to the work at Strasbourg/DAPNIA and LBNL/Berkeley, efforts are under way at Yale/Oregon, in the U.K. (LCFI Collaboration), and probably others of which the proposer is unaware as they did not make presentations at either ILC Snowmass 2005 or PIXEL2005.


[13] Extrapolating background hit estimates from silicon strips to MAPS depends strongly on the charged particle to x-ray/γ ratio. For CAPS, the pixel is about 8,000 times smaller, has an 9 times longer integration time and the active volume is about 30 times smaller than the reference silicon strip. At 20 times background, the 10% DSSD occupancy becomes ∼ 7.5 × 10−3% for all neutral and ∼ 0.225% for all charged tracks.


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