

XFT RX Pulsar Board

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This document describes the XFT Rx Pulsar board and its firmware for the L2 trigger upgrade. It is a synthesis of the information in the XFT section (Section 2.2.5) of the “Pulsar Firmware for L2 trigger upgrade” document and the “XFT Firmware Modifications” document written in July of 2007.

1. Functionality Overview

The XFT Rx Interface Board receives data sent from the L1 XFT Finder boards. The data is recorded in DAQ RAMs, merged into one package, and sent out in the Pulsar S-LINK format.

XFT data comes into the board on 12 fibers. The XFT input interface is through the XFT receiver mezzanine cards on the Pulsar board. One XFT receiver mezzanine card sinks data from three fibers. With four mezzanine cards, the board can sink data from 12 XFT fibers. Two mezzanine cards are connected to each DataIO FPGA. XFT input data is saved in DAQ RAM 1 on the DataIO FPGAs. Data received by the DataIO FPGAs is merged and sent to the Control FPGA, along with the data word counts for each Finder channel.

In the Control FPGA, the data from the DataIO FPGAs is merged again, and the Finder channel word counts are inserted at the end of the data packet. A fast abort signal, generated by the Tracklist Pulsar board, signals the XFT firmware to abort the current event, resulting in the transmission of a single data word. Word counters and timers in the Control FPGA monitor events, predict possible overflows of the downstream FILAR FIFOs, and truncate such events. The final event data is sent out through the P3 connector. Outgoing data has the Buffer number, seen by the XFT interface board for the current event, and the Bunch counter value, counted by the board, in the S-LINK header word. Also, the data source value is set accordingly in the S-LINK header word (See Appendix 2 of the “Pulsar Firmware for L2 trigger upgrade” document). The outgoing data is saved in DAQ RAM 1 of the Control FPGA.

From P3, the S-LINK formatted data goes out through the S-LINK LSC mezzanine card on the Pulsar AUX card.

Input latency from L1A to the arrival of XFT data on an input is measured for each input.

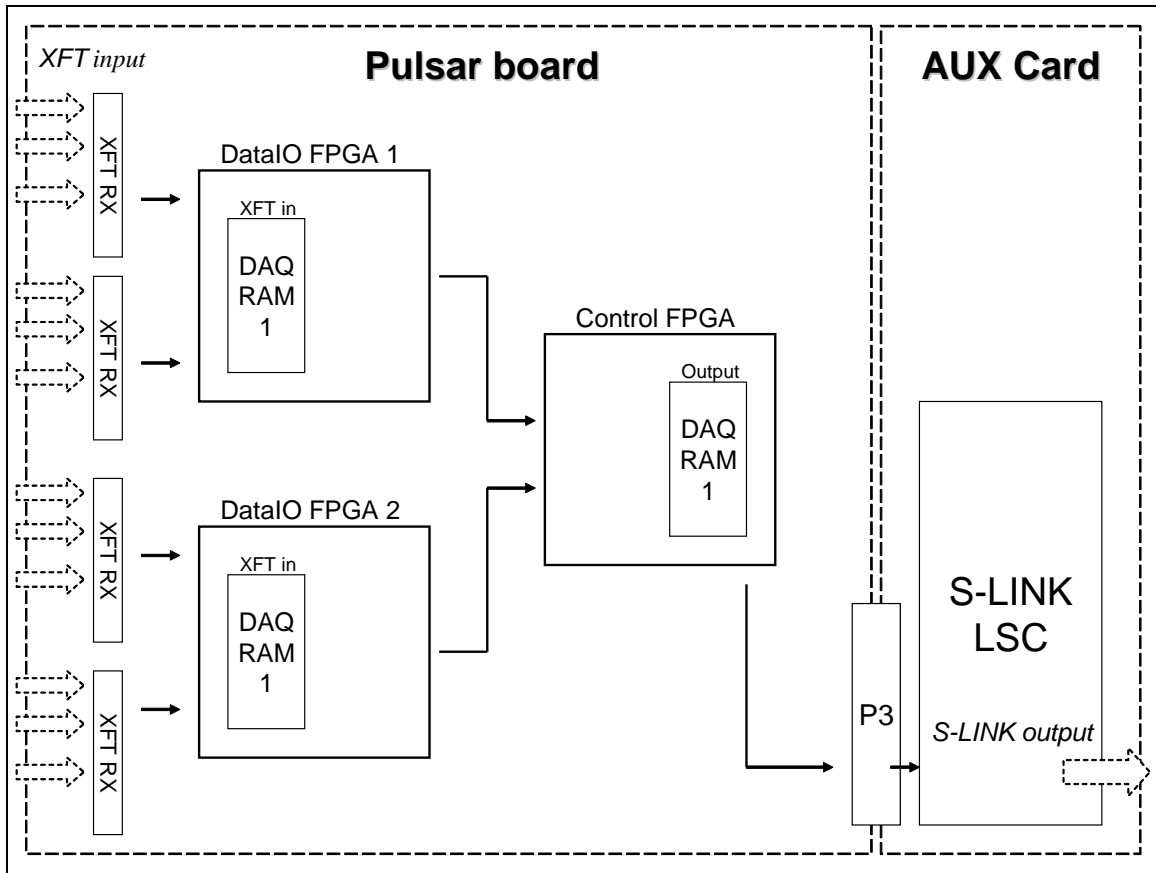


Figure 1: XFT Rx Interface board overview.

2. General Specs for Pulsar Firmware

This section is a summary of the requirements for Pulsar firmware described in the note titled, "Pulsar Firmware for L2 trigger upgrade."

a. Register Space

All VME interface components have three status registers (read only), four control registers (read/write), and two pulse registers (write only). These registers are used differently in different firmware, but the first two registers are reserved. The first status register has a firmware version value in it. The first pulse register is used to reset the FPGA.

DataIO FPGA 1

Name	Address	Type
Firmware version	YY080000	R
Reset	YY080004	W
Control register 1	YY080008	R/W
Control register 2	YY08000C	R/W
Status register 1	YY080010	R
Pulse 1	YY080014	W
Control register 3	YY080018	R/W
Control register 4	YY08001C	R/W
Status register 2	YY080020	R

DataIO FPGA 2

Name	Address	Type
Firmware version	YY0C0000	R
Reset	YY0C0004	W
Control register 1	YY0C0008	R/W
Control register 2	YY0C000C	R/W
Status register 1	YY0C0010	R
Pulse 1	YY0C0014	W
Control register 3	YY0C0018	R/W
Control register 4	YY0C001C	R/W
Status register 2	YY0C0020	R

Control FPGA

Name	Address	Type
Firmware version	YY000000	R
Reset	YY000004	W
Control register 1	YY000008	R/W
Control register 2	YY00000C	R/W
Status register 1	YY000010	R
Pulse 1	YY000014	W
Control register 3	YY000018	R/W
Control register 4	YY00001C	R/W
Status register 2	YY000020	R

YY = VME address bits 31..24,
not used by the firmware.

Table 1: VME interface registers

b. DAQ RAMs

Each FPGA has two DAQ RAMs. We have chosen this implementation so that the interface to the DAQ RAMs is identical to all Pulsars and to all FPGAs. However, in some cases, none, or only one of them, is actually used. For example, in the Pulsar SVT board, the DAQ RAMs in the DataIO FPGAs are always empty. The SVT board only uses the two DAQ RAMs in the Control FPGA.

We have labeled the first DAQ RAM on an FPGA as DAQ RAM 1 and the second as DAQ RAM 2. Each DAQ RAM is divided into four buffers corresponding to the four L2 DAQ buffers. To each buffer a word count register is associated, which indicates the number of words in that buffer.

Each buffer can also be subdivided. For example, one DAQ RAM can have data from eight different inputs. The use of the DAQ RAMs in different firmware is described in more detail in the “Pulsar Firmware for L2 trigger upgrade” document.

The VME interface component uses the VME address bits to determine which DAQ RAM is being read out and enables that DAQ RAM’s output to the VME data bus. Also, the word count registers are enabled to the VME data bus the same way.

When reading out DAQ RAMs, VME address bit 17 chooses between the DAQ RAMs inside one FPGA.

VME address bit Selected DAQ RAM

17	
0	DAQ RAM 1
1	DAQ RAM 2

Table 2: VME address bit for DAQ RAM selection

When reading out DAQ RAMs, VME address bit 23 is set high, bit 22 is set low, and bits 20 and 21 select which buffer is read out. This follows the CDF specification for DAQ readout defined in CDF note 2388.

VME address bit Selected buffer

23 22 21 20				
1	0	0	0	Buffer 0
1	0	0	1	Buffer 1
1	0	1	0	Buffer 2
1	0	1	1	Buffer 3

Table 3: VME address bits for DAQ RAM buffer selection

VME addresses for the word count registers are listed in Table 4 below. Some firmware has more than one word count register per DAQ RAM.

DataIO FPGA 1

DAQ RAM	Buffer #	Address
1	0	YY080800
1	1	YY080900
1	2	YY080A00
1	3	YY080B00
2	0	YY080804
2	1	YY080904
2	2	YY080A04
2	3	YY080B04

DataIO FPGA 2

DAQ RAM	Buffer #	Address
1	0	YY0C0800
1	1	YY0C0900
1	2	YY0C0A00
1	3	YY0C0B00
2	0	YY0C0804
2	1	YY0C0904
2	2	YY0C0A04
2	3	YY0C0B04

Control FPGA

DAQ RAM	Buffer #	Address
1	0	YY000800
1	1	YY000900
1	2	YY000A00
1	3	YY000B00
2	0	YY000804
2	1	YY000904
2	2	YY000A04
2	3	YY000B04

YY = VME address bits 31..24,
not used by the firmware.

Table 4: Word count register VME addresses

In the beginning of each buffer of DAQ RAM 1 in the Control FPGA, there is a DAQ Header Word. The format follows CDF note 2388. Currently, Pulsar firmware does not provide Geographical Address in the DAQ Header Word.

Bit	Description
0..7	Bunch Counter Value
8..12	Geographical Address
13..22	Board Serial Number
23..31	Board Type

Table 5: DAQ Header Word format

c. IDPROM

All Control FPGAs have a read-only memory that contains the values of an IDPROM. IDPROM format is also defined in CDF note 2388.

For all Control FPGA firmware, an IDPROM is included in the VME interface. The IDPROM read-only memory values are in a memory input file (.mif), which is taken in into compilation when compiling the firmware.

d. Board Type

Each Pulsar board has been assigned its own Board type. The Board type value is put into the IDPROM, DAQ header word, and the S-LINK data stream as part of a header word. Board type is used to distinguish data from different Pulsar boards in the trigger system.

Board type	Description
081	L2 Pulsar Muon/XTRP Rx IIa
083	L2 Pulsar SVT Road Warrior
085	L2 Pulsar Muon/XTRP/L1 Tx or SVT XTRP-emu
086	L2 Pulsar Muon/XTRP/L1 Rx IIb
087	L2 Pulsar SHOWERMAX Tx
088	L2 Pulsar SHOWERMAX Rx
089	L2 Pulsar Cluster/PreFred Tx
090	L2 Pulsar Cluster/PreFred Rx
091	L2 Pulsar SVT Tx
092	L2 Pulsar SVT Rx
093	L2 Pulsar Merger Tx
094	L2 Pulsar Merger Rx
095	L2 Pulsar L2TS Tx
096	L2 Pulsar L2TS
097	L2 Pulsar L1 Scaler
098	L2 Pulsar SVT TF
099	L2 Pulsar test one
100	L2 Pulsar test two
101	L2 Pulsar Stereo Tx
102	L2 Pulsar Stereo Rx (XFT Rx)
103	SVT Pulsar Hit Buffer
107	Tracklist A
108	Tracklist B
109	12Cal Pulsar

Table 6: Pulsar Board types

3. DataIO FPGA Firmware

The firmware for both DataIO FPGAs is identical (see Figure 2 for a block diagram). Two XFT receiver mezzanine cards, each of which has three of its four fiber inputs populated, connect to each DataIO FPGA (for a total of 12 channels between both FPGAs). The data from all 6 Finder channels is merged, channel word counts are inserted into the data stream, and a single data packet is sent to the Control FPGA.

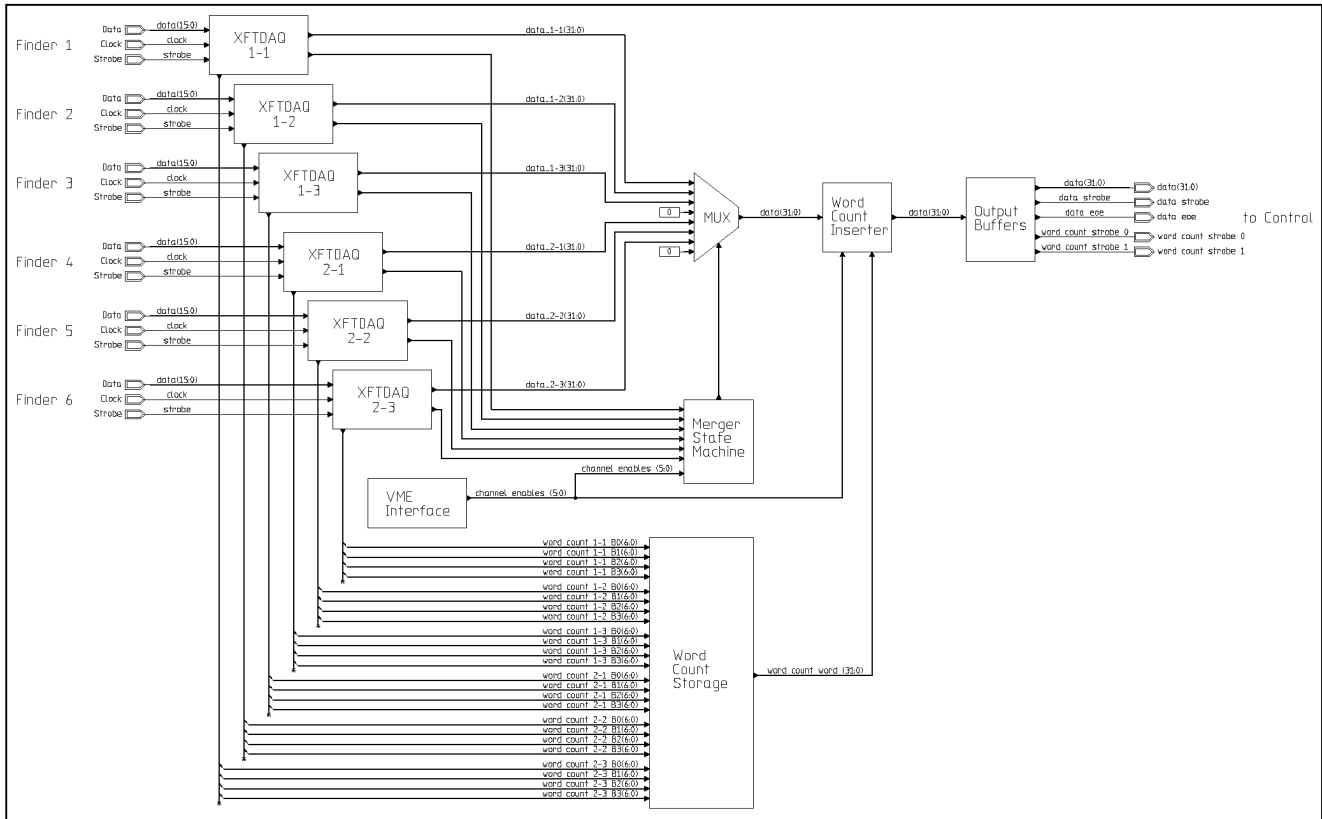


Figure 2: Overview block diagram of the XFT DataIO FPGA firmware.

a. Inputs to DataIO FPGAs

The 16-bit XFT communication protocol is used for transferring data from the Finders to the XFT Pulsar. Under this protocol, the first word of each data packet has bits 15:14 set to 10_2 , and the last word of each data packet has bits 15:14 set to 11_2 , with all data words having bit 15 set low.

b. Functionality of DataIO FPGAs

Each Finder channel is connected to its own XFTDAQ component (see Figure 3 for a diagram). A 32-words deep 16-bit input FIFO is used to receive the XFT data. With State Machine 1 (see Figure 4) and two 16-bit registers, 32-bit words are formed from the incoming 16-bit words. State Machine 1 writes the 32-bit words into an input DAQ

RAM and to an output FIFO. An L1A FIFO, strobed on each L1A, is used to save the Buffer number for the incoming events. State Machine 1 also controls a write address counter, the output of which is used as part of the write address for the input DAQ RAM. The buffer number controls the upper two bits of the write address. This way, the RAM is divided into four buffers. Input DAQ RAMs are 512 words deep, so there are 128 words per buffer. See Section 5 for details how each input DAQ RAM is mapped to VME.

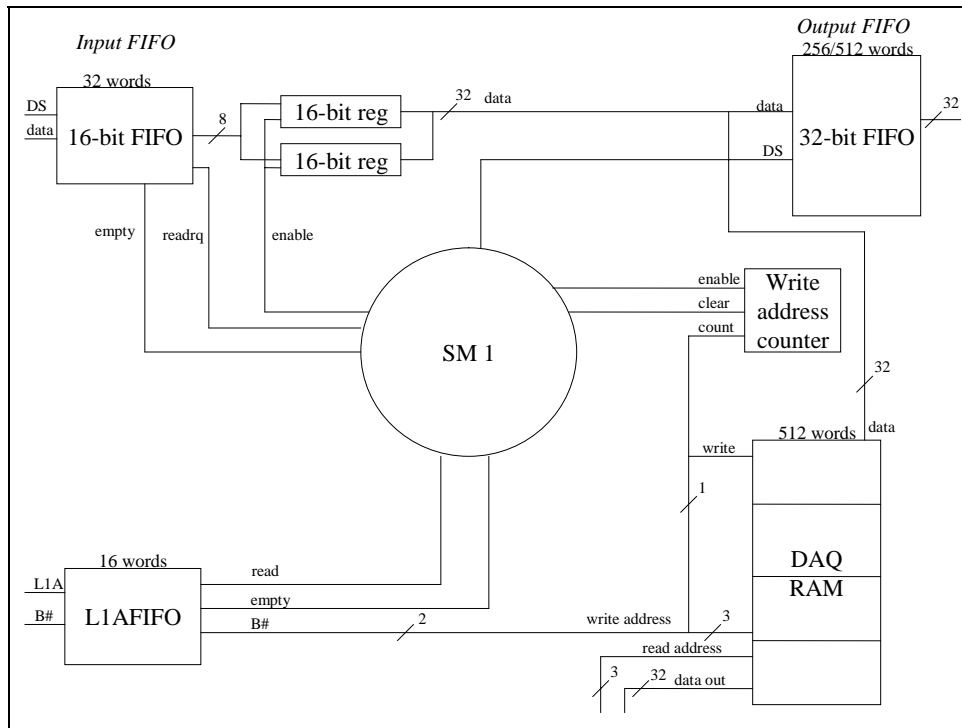


Figure 3: Block diagram of the XFTDAQ component of the DataIO firmware.

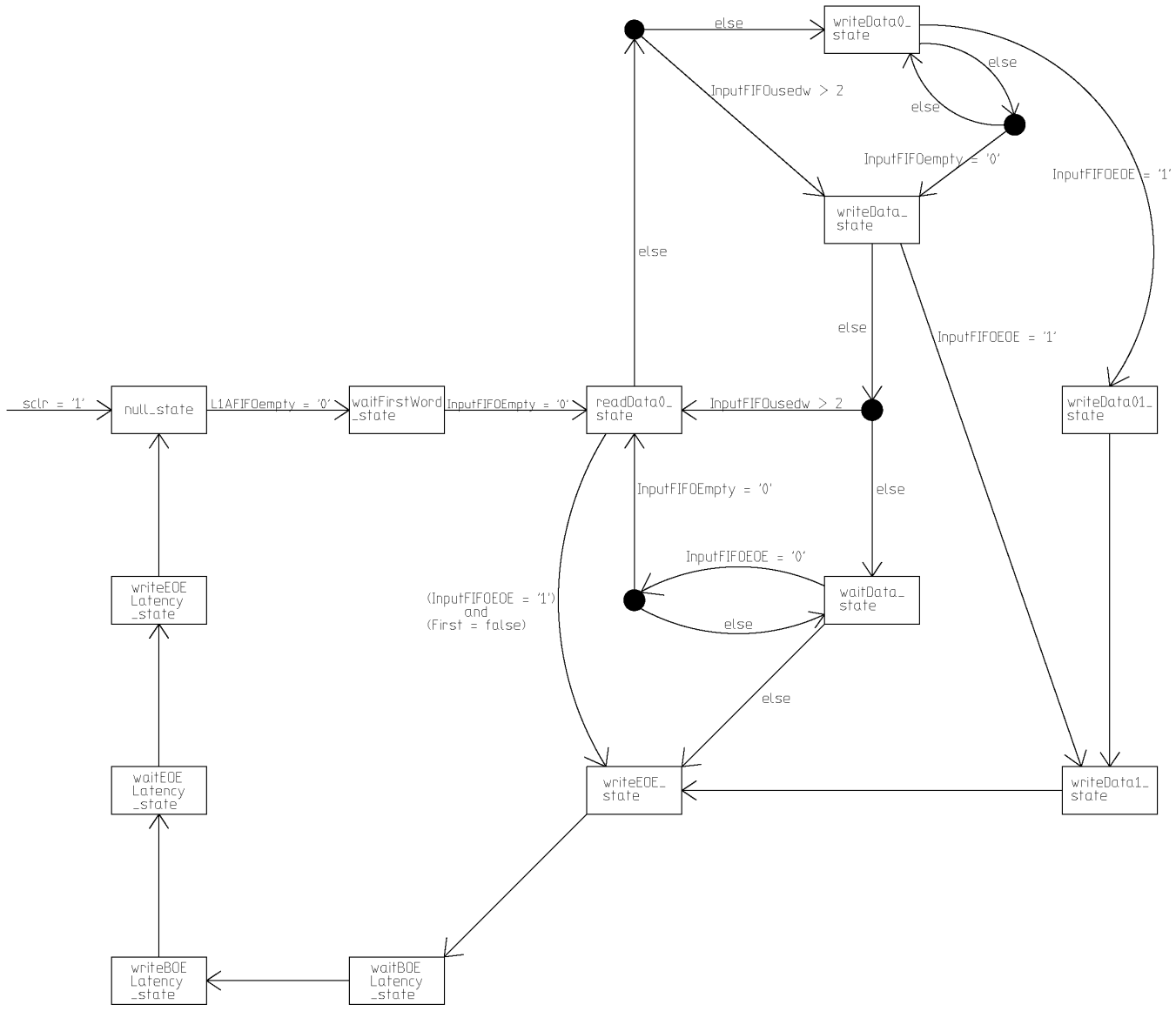


Figure 4: Diagram of State Machine 1 in the XFTDAQ component.

The output FIFOs for each channel are read by the Merger State Machine (see Figure 5), which merges the data and sends them out to the Control FPGA. Data from the first input component (the first channel on the first mezzanine card, which is connected to XFTDAQ 1-1) is sent out first, data from the second input component next (XFTDAQ 1-2), and so on.

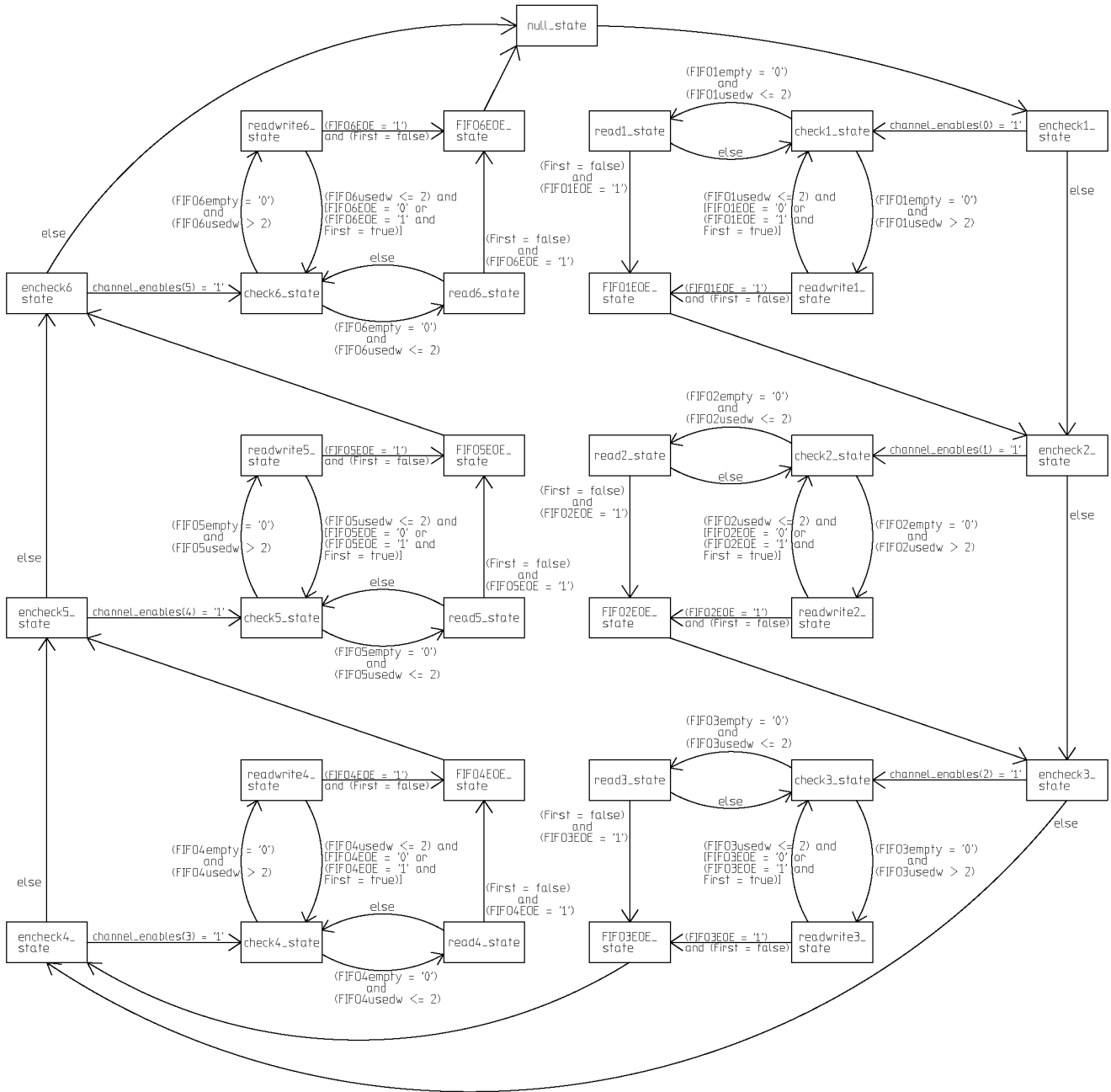


Figure 5: Diagram of the Merger State Machine in the DataIO FPGA firmware.

Six channel enable bits, set in Control Register 1 of the VME Interface, tell the Merger State Machine which channels are enabled. Each bit corresponds to one Finder channel as shown in Table 7. A bit value of 1 enables each channel, and the power-up setting for these bits is 111111_2 . Note that after changing the value of this register, the FPGA firmware must be reset to guarantee proper functioning of the state machines. Also note that the firmware is not designed to handle the case in which all 6 channels are disabled.

Channel Enable Bit (Control Register 1)	Finder Channel
0	Mezzanine Card 1, Channel 1
1	Mezzanine Card 1, Channel 2
2	Mezzanine Card 1, Channel 3
3	Mezzanine Card 2, Channel 1
4	Mezzanine Card 2, Channel 2
5	Mezzanine Card 2, Channel 3

Table 7: Correlation between the Finder channels and the channel enable bits of Control Register 1.

Once the data from all six channels has been merged, the word counts for each Finder channel for the current event are appended to the end of the data packet in two 32-bit words (see Table 8 for the formats). Word 1 is sent on the clock cycle immediately following the second EOE word, and Word 2 is sent on the clock cycle after Word 1. Word counts for all disabled channels are set to zero.

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word 1	0	0	Word Count Chan. 4						Word Count Chan. 3						0	0	Word Count Chan. 2						Word Count Chan. 1									
Word 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Word Count Chan. 6						Word Count Chan. 5							

Table 8: Format of the words containing Finder word counts.

The DataIO FPGA firmware uses the latency-measuring component to measure latency from L1A to when the data starts arriving at an input and when the whole XFT event is received. Measuring is based on the SLINK40MHzClk, and an increase of one in the latency value represents 100ns. These latency measurement values are stored after the data at the end of each channel's input DAQ RAM for all four buffers.

c. Outputs of DataIO FPGAs

The output interface to the Control FPGA consists of 32 data lines, a data strobe, two word count strobes, and a data EOE line. See Table 9 for an example of the transmission for an event.

Data (32 bits)	Data Strobe	Data EOE	Word Count 1 Strobe	Word Count 2 Strobe
Channel 1 Data Word 1	1	0	0	0
...	1	0	0	0
Channel 1 Data Word N_1 (EOE)	1	0	0	0
Channel 2 Data Word 2	1	0	0	0
...	1	0	0	0
Channel 2 Data Word N_2 (EOE)	1	0	0	0
...	1	0	0	0
Channel 6 Data Word N_6-1	1	0	0	0
Channel 6 Data Word N_6 (EOE)	1	1	0	0
Channel 6 Data Word N_6 (EOE)	1	1	0	0
Word Count Word 1	0	0	1	0
Word Count Word 2	0	0	0	1

Table 9: Transmission of a typical event to the Control FPGA with the corresponding control signal values. All 6 input channels are enabled. There will be some clock cycles between the data words during which nothing is transmitted (all control signals are low).

All data words for the first channel are sent, ending with an end-of-event word for that channel. Then all the data words are sent for the second channel, etc. The last word of the last channel is repeated, and the Data EOE control signal is high for both words. The word counts are transmitted during the two clock cycles immediately after the Data EOE. For these two words, only their respective strobes are high.

4. Control FPGA Firmware

The Control FPGA firmware receives data and word counts from both DataIO FPGAs, merges them, checks for aborted events and possible overflow of the FILAR FIFOs, then sends the data packet to a FILAR board over an S-LINK connection. Figure 4 shows a block diagram of the firmware's main functionality.

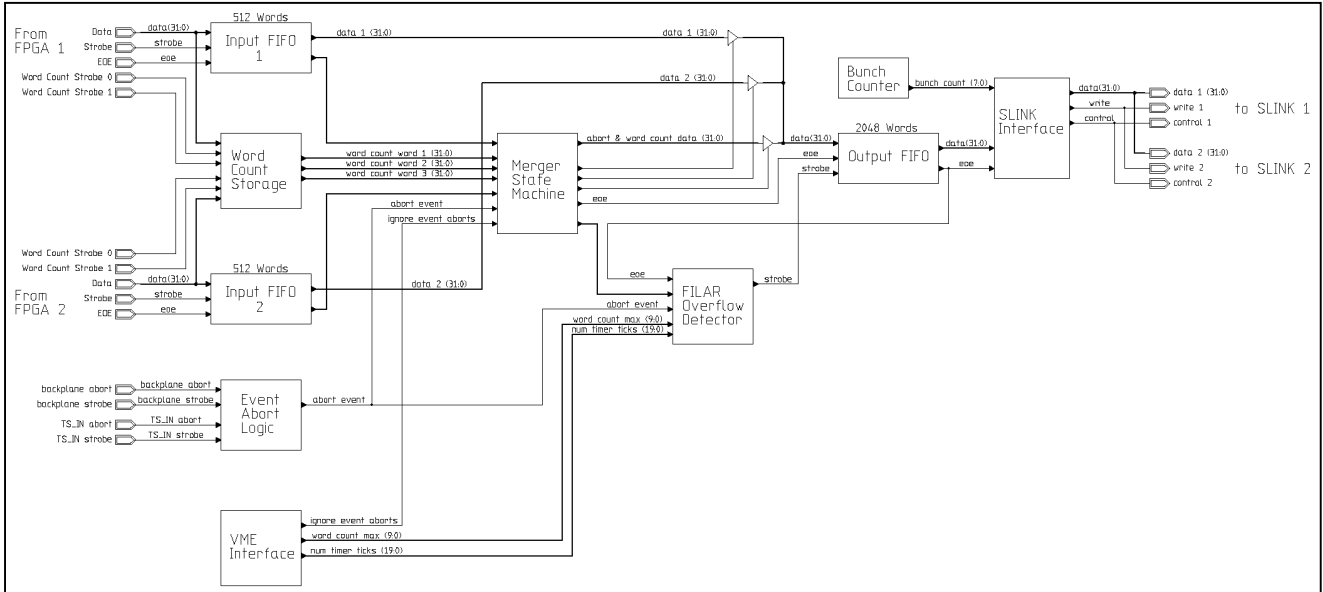


Figure 4: Overview block diagram of the XFT Control FPGA firmware.

a. Inputs to Control FPGA

The Control FPGA receives data from the two DataIO FPGAs in the format described in Table 9. It also receives an event abort signal from the Tracklist A Pulsar board, which is used to prevent the transmission of data from unwanted events. This abort signal and accompanying strobe can be received either through the P2 backplane connector (if the XFT Rx board is in the same crate as the Tracklist A board) or from an LVDS cable connected to TS_Out on the front panel of the Pulsar board. See Table 10 for the connector pinouts and Figure 5 for a timing diagram of the abort signals.

The firmware automatically detects which connector is used for receiving the abort signal. However, it is important that both are not used simultaneously, or else too many abort signals will be received. Therefore, if an XFT Rx board is in the same crate as the Tracklist A board, nothing should be connected to TS_Out.

	P2 Connector			TS_OUT Connector		
	Pin Name	Logic Type	Pin #	Pin Name	Logic Type	Pin #
Abort Data	PULSAR_FREEZE*	TTL	A3	TS_OUT(0) +	LVDS	3
				TS_OUT(0) -	LVDS	4
Abort Strobe	PULSAR_SPARE*	TTL	A5	TS_OUT(1) +	LVDS	5
				TS_OUT(1) -	LVDS	6

Table 10: Event abort signal pinouts for the Pulsar board TS_Out and P2 connectors.

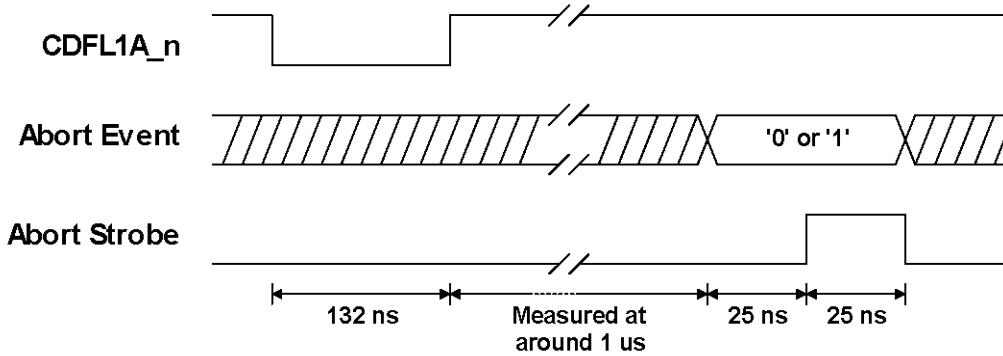


Figure 5: Timing diagram of the event abort signal and accompanying strobe.

b. Functionality of Control FPGA

For each event, the data from each DataIO FPGA is stored in an input FIFO, which is 512 words deep. The two words containing Finder word counts from each DataIO FPGA, sent after the EOE word of each data packet, are merged into three words (see Table 11 for the formats) and stored. An abort signal, sent by the Tracklist A Pulsar board, is also recorded.

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word 1	0	0	Word Count Chan. 4				Word Count Chan. 3				0	0	Word Count Chan. 2				Word Count Chan. 1															
Word 2	0	0	Word Count Chan. 8				Word Count Chan. 7				0	0	Word Count Chan. 6				Word Count Chan. 5															
Word 3	0	0	Word Count Chan. 12				Word Count Chan. 11				0	0	Word Count Chan. 10				Word Count Chan. 9															

Table 11: Format of the words containing Finder word counts after merging the word counts from both DataIO FPGAs.

Once the abort signal has been registered, the Merger State Machine (see Figure 6 for a diagram) pulls data out of the input FIFOs, appends the three Finder-word-count words, and sends the data packet to the 2048-word Output FIFO. If the event was aborted, then the word counts are not sent, and only one data word is transmitted: 0xC000C000.

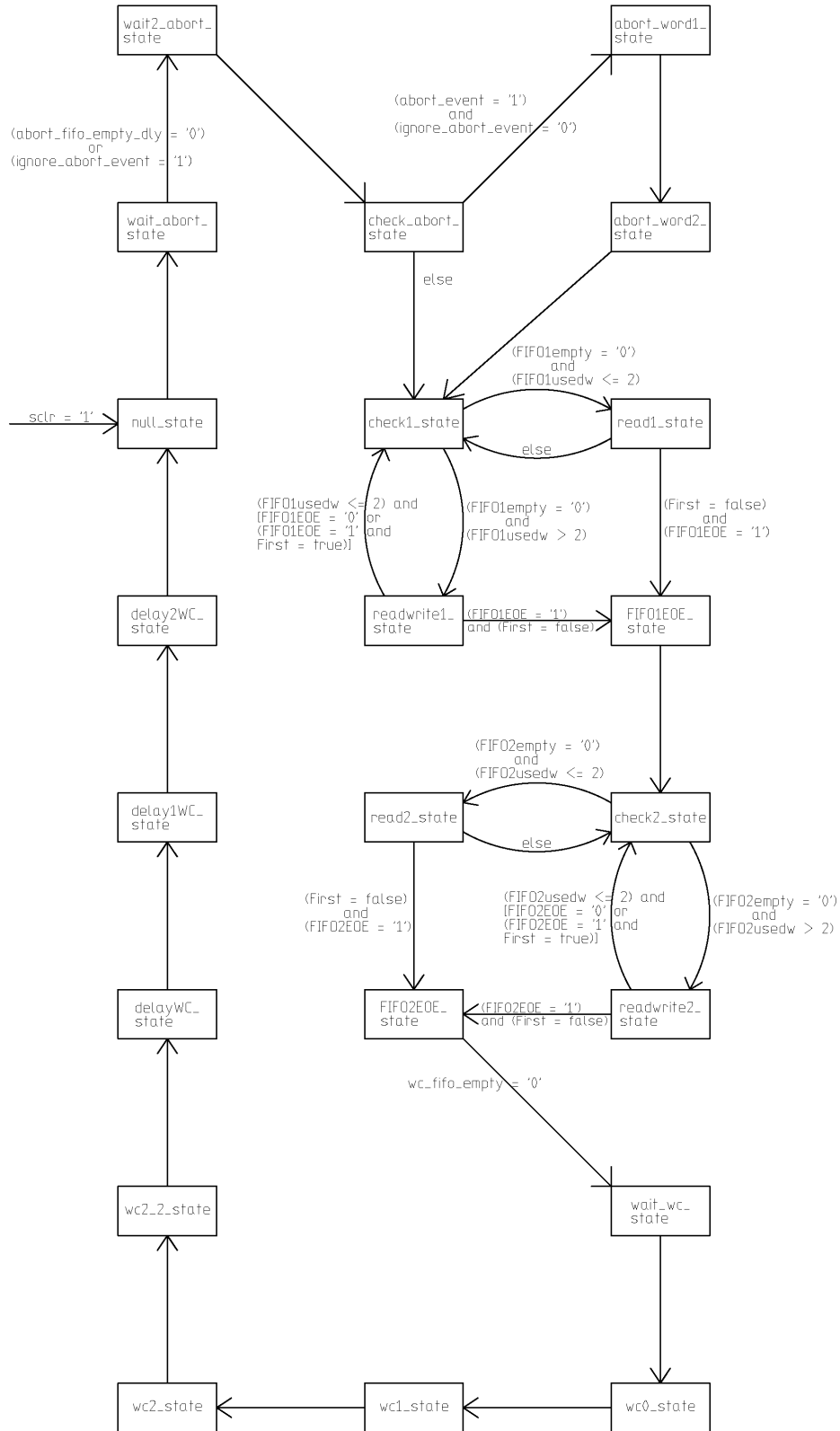


Figure 6: Diagram of the Merger State Machine in the Control FPGA firmware.

While the data words are merged by the Merger State Machine, they are counted by the FILAR Overflow Detector (see Figure 7 for a block diagram). At the end of each event, or when an overflow occurs, the current word count is stored in one of four registers. When this happens, a timer associated with that register begins counting (it increments every 12.5 ns). When that timer reaches the 20-bit “num timer ticks” value (stored in bits 19:0 of Control Register 3), the register is cleared.

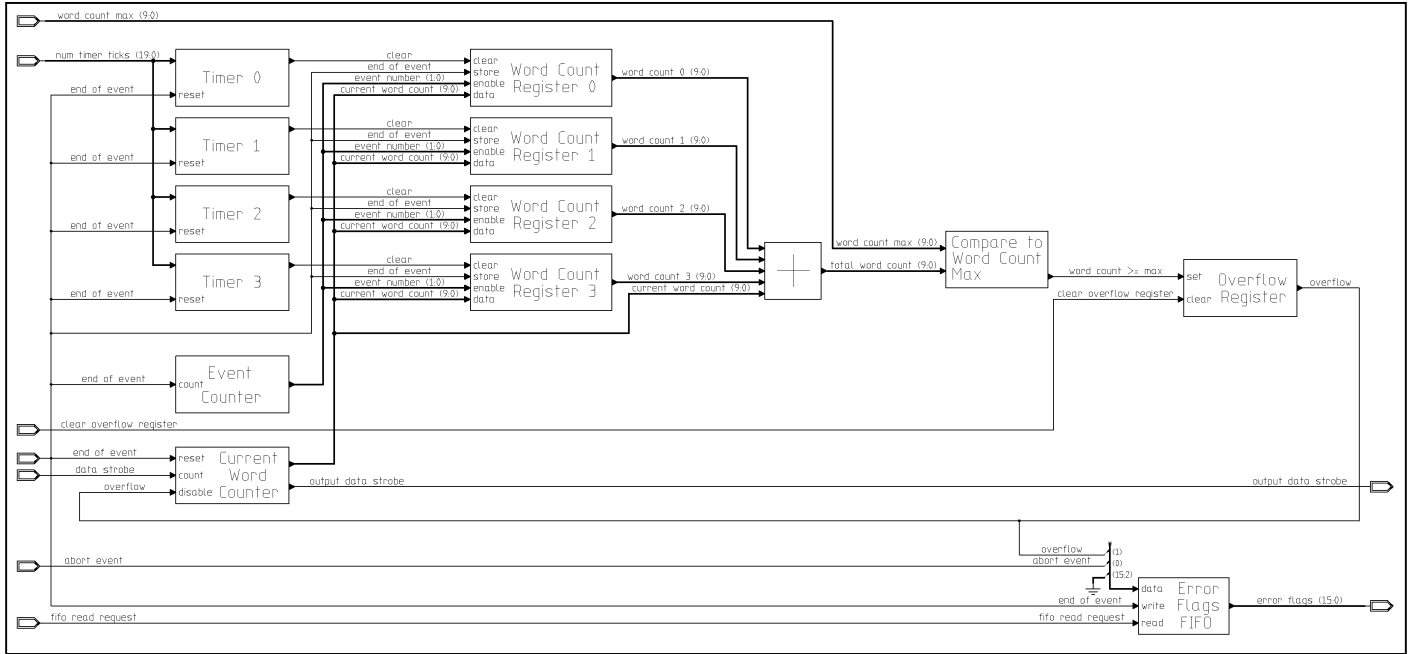
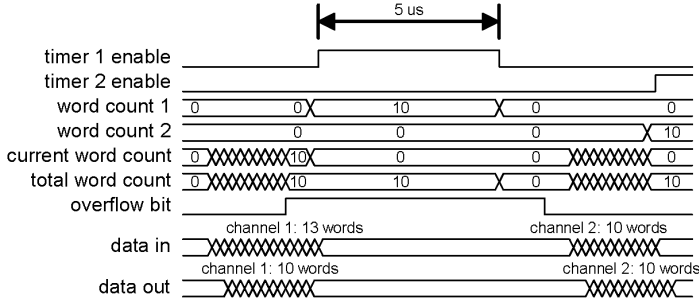


Figure 7: Overview block diagram of the FILAR Overflow Detector in the Control FPGA firmware. Data words are dropped by masking out the output data strobe.

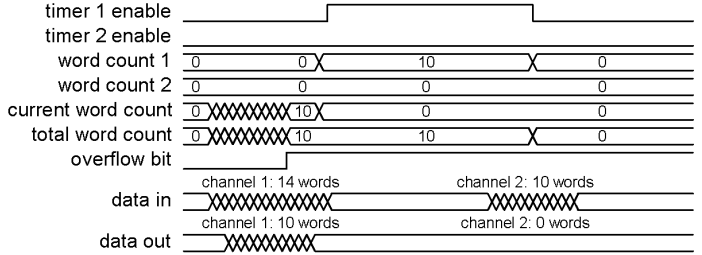
If, at any time, the sum of the current word count and the four word count registers is greater than or equal to the 10-bit “word count max” value (stored in bits 29:20 of Control Register 3), an overflow occurs (see Figure 8 for examples of how this works) and the truncation flag is set in the S-LINK trailer word (see Section 4c: “Outputs of Control FPGA”). The current event is truncated, meaning that no more data words are sent—only the Finder-word-count words and the words that end the S-LINK packet. Until the total word count drops below “word count max,” future packets will also be truncated. Note that if the overflow condition disappears in the middle of transmitting an event, that event will still be truncated (the overflow flag is only allowed to reset between events). Also note that only data words are counted, not the Finder-word-count words or any of the S-LINK words. These “extra” words should be taken into account when setting the maximum word count value.

For all 6 cases: Word Count Max = 10, Timer Delay = 5us
 Meaning, all "timer # enable" signals will be high for 5 us

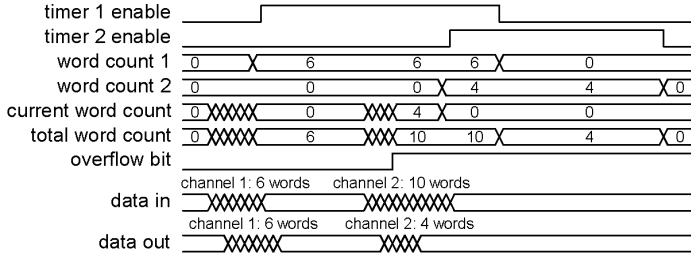
Case 1: Overflow from channel 1, cleared for channel 2



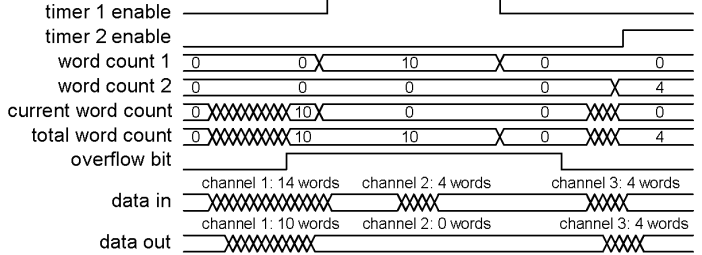
Case 4: Overflow from channel 1, continued partly through channel 2



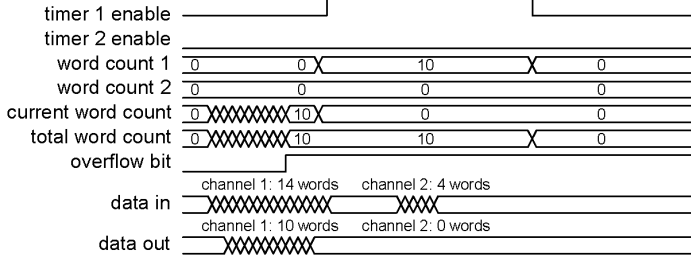
Case 2: Overflow from channel 2



Case 5: Overflow from channel 1, continued through channel 2, cleared for channel 3



Case 3: Overflow from channel 1, continued through channel 2



Case 6: No overflow until channel 3

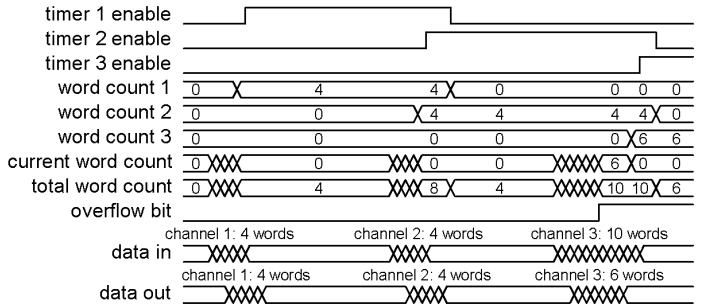


Figure 8: Examples of how overflow detection works. This is not a list of all possible cases. There are 4 timers and 4 word count registers in the firmware. “Data in” and “data out” in these timing diagrams are only for the FILAR Overflow Detector, not the entire FPGA design, so they do not include any of the Finder-word-count words or S-LINK header and trailer words. The exact timing and word counts may be off a little due to delays. See Table 12 for greater precision. Note that the overflow bit (which causes events to be truncated when set) does not reset until a few clock cycles before the beginning of the next event that should *not* be truncated. Also note that the “current word count” does increment on each input data word. The value is immediately stored in a “word count #” register and cleared once the input packet is complete, which is why “current word count” is sometimes equal to 0 in the gaps.

Because there is a delay of two clock cycles between counting a word and setting the overflow flag in the FILAR Overflow Detector, there are a few different scenarios that can occur if the number of data words is close to the set maximum. Table 12 gives an example.

# Input Words			# Transmitted Words			Truncation/Overflow Results		
Data	FWCs	Total	Data	FWCs	Total	Truncation	Truncation Flag Set	Overflow Set for Future
1	3	4	1	3	4	No	No	No
2	3	5	2	3	5			
3	3	6	3	3	6			
4	3	7	4	3	7			
5	3	8	5	3	8			
6	3	9	6	3	9			
7	3	10	7	3	10			
8	3	11	8	3	11			
9	3	12	9	3	12			
10	3	13	10	3	13			
11	3	14	11	3	14	Yes	Yes	
12	3	15	12	3	15			
13	3	16	12	3	15			
14	3	17	12	3	15			
15	3	18	12	3	15			

Table 12: Example of the number of words transmitted for different numbers of input data words. The word count maximum is set to 10. FWC = Finder Word Count.

The functionality of the FILAR Overflow Detector is designed to approximately emulate the filling and draining of the 512-word FILAR input FIFOs. The idea is to prevent the transmission of too many data words, which would cause those FIFOs to overflow. Data sits in the FILAR FIFOs for a period of time—represented by the timers—and then drains quickly, which is represented by the clearing of the word count registers.

c. Outputs of Control FPGA

Once data has been stored in the Output FIFO, it is drained by the SLINK Interface. Here, it is converted to the Pulsar S-LINK format, stored in DAQ RAM 1 (which is 2048 words deep, or 512 per buffer), and sent out to a FILAR board. See Tables 13-15 for details of the S-LINK transmission.

No Abort, No Truncation	No Abort, Truncation	Abort, With or Without Truncation
SLINK BOF	SLINK BOF	SLINK BOF
SLINK Header 1	SLINK Header 1	SLINK Header 1
SLINK Header 2	SLINK Header 2	SLINK Header 2
Data Packet Word 1	Data Packet Word 1	0xC000C000
...	...	SLINK Trailer Word
Data Packet Word N (Data Packet Trailer Word)	Data Packet Word T (last data word; likely not data packet trailer word)	SLINK EOF
Finder Word Counts 1	Finder Word Counts 1	
Finder Word Counts 2	Finder Word Counts 2	
Finder Word Counts 3	Finder Word Counts 3	
SLINK Trailer Word	SLINK Trailer Word	
SLINK EOF	SLINK EOF	

Table 13: Structure of the Pulsar XFT Rx board data sent to L2 via S-LINK. The output is given for all combinations of event abort and event truncation. The DAQ header word and various S-LINK control word definitions are given in Table 14.

Data Word	Bit Definition
DAQ Header Word	Board Type (31:23), Serial Number (22:13), Reserved (12:8), Bunch Counter (7:0)
SLINK BOF	SLINK Beginning of Fragment Control Word (0xB0F00000)
SLINK Header 1	Format (31:24), Source (23:20), Region ID (19:18), Reserved (17:10), Bunch Counter (9:2), L2 Buffer Number (1:0)
SLINK Header 2	Reserved (31:16), Latency (15:0)
SLINK Trailer	Data Size (31:16), Error Flags (15:0)
SLINK EOF	SLINK End of Fragment Control Word (0xE0F00000)

Table 14: Header word and S-LINK control word definitions for the Pulsar XFT Rx board. The S-LINK trailer word error flag definitions are given in Table 15.

Bit	Definition
0	Abort (event was aborted by the Tracklist board)
1	Truncation (event was truncated to prevent FILAR overflow)
2	Ignoring Aborts (firmware is currently ignoring event aborts)
15:3	All 0s

Table 15: Bit assignments for the Error Flags in the S-LINK Trailer word.

5. Register Space

Table 16 summarizes the register space of all three FPGAs. Tables 17 and 18 provide more details about the two State Registers in the Control FPGA firmware.

DataIO FPGA 1

Name	Address	Description	Databits	Data
Firmware Version	YY080000 (R)	Firmware version	31...0	0x0D705140
Reset	YY080004 (W)	Reset FPGA	-	-
DAQ SW Version	YY080008 (R/W)	DAQ SW version	31...0	Power-up value: 0
Control Register 1	YY08000C (R/W)	Channel enables	5...0	Power-up value: 0x3F
Status Register 1	YY080010 (R)	Not used	31...0	0x00C0FFEE
Pulse 1	YY080014 (W)	Not used	-	-
Control Register 2	YY080018 (R/W)	Not used	31...0	Power-up value: 0
Control Register 3	YY08001C (R/W)	Not used	31...0	Power-up value: 0
Status Register 2	YY080020 (R)	Not used	31...0	0x00000CDF

DataIO FPGA 2

Name	Address	Description	Databits	Data
Firmware Version	YY0C0000 (R)	Firmware version	31...0	0x0D705140
Reset	YY0C0004 (W)	Reset FPGA	-	-
DAQ SW Version	YY0C0008 (R/W)	DAQ SW version	31...0	Power-up value: 0
Control Register 1	YY0C000C (R/W)	Channel enables	5...0	Power-up value: 0x3F
Status Register 1	YY0C0010 (R)	Not used	31...0	0x00C0FFEE
Pulse 1	YY0C0014 (W)	Not used	-	-
Control Register 2	YY0C0018 (R/W)	Not used	31...0	Power-up value: 0
Control Register 3	YY0C001C (R/W)	Not used	31...0	Power-up value: 0
Status Register 2	YY0C0020 (R)	Not used	31...0	0x00000CDF

Control FPGA

Name	Address	Description	Databits	Data
Firmware Version	YY000000 (R)	Firmware version	31...0	0x0C710090
Reset	YY000004 (W)	Reset FPGA	-	-
DAQ SW Version	YY000008 (R/W)	DAQ SW version	31...0	Power-up value: 0
Control Register 1	YY00000C (R/W)	Bunch Count Shift	7...0	Power-up value: 41
Status Register 1	YY000010 (R)	Not used	31...0	0x00C0FFEE
Pulse 1	YY000014 (W)	Not used	-	-
Control Register 2	YY000018 (R/W)	Ignore aborts	0	Power-up value: 1
Control Register 3	YY00001C (R/W)	Word count max.	29...20	Power-up value: 1023
		Timer delay	19...0	Power-up value: 16
Status Register 2	YY000020 (R)	Not used	31...0	0xDEADBEEF
State Register 1	YY000024 (R)	Truncation state	31...0	
State Register 2	YY000028 (R)	Truncation state	31...0	
IDPROM	YY100000 – YY10007C (R)	ID PROM	31...24	

Table 16: XFT Rx Pulsar Board register space for all three FPGAs.

Bits	Definition
31:30	“00”
29:20	Word Count Register 1 (9:0)
19:10	Word Count Register 0 (9:0)
9:0	Current Word Count (9:0)

Table 17: Bit definitions of State Register 1 in the Control FPGA.

Bit(s)	Definition
31:28	“0000”
27	Timer 3 Enable
26	Timer 2 Enable
25	Timer 1 Enable
24	Timer 0 Enable
23:22	Event Count (1:0)
21	Total Word Count \geq Word Count Max.
20	Overflow Bit
19:10	Word Count Register 3 (9:0)
9:0	Word Count Register 2 (9:0)

Table 18: Bit definitions of State Register 2 in the Control FPGA.

6. RAM and FIFO Size Summary

Table 19 summarizes the sizes of the RAMs and FIFOs in the firmware.

DataIO FPGA	Control FPGA
One XFT Channel (6/DataIO FPGA) has: <ul style="list-style-type: none"> • Input FIFO: 32 words x 16 bits • Output FIFO: <ul style="list-style-type: none"> ○ First Channel: 256 words x 32 bits ○ Other Channels: 512 words x 32 bits • Input DAQ RAM: 512 words x 32 bits (128 words/buffer) 	<ul style="list-style-type: none"> • 2 Input FIFOs: 512 words x 32 bits • Output FIFO: 2048 words x 32 bits • Output DAQ RAM: 2048 words x 32 bits (512 words/buffer)

Table 19: RAM and FIFO sizes in the XFT Rx Pulsar board firmware.