

XFT VME addresses

DataIO FPGA 1

Name	Address	Description	Databits	Data
Firmware version	YY080000 (R)	Firmware version	31...0	0x0d509190
Reset	YY080004 (W)	Reset FPGA	-	-
DAQ SW version	YY080008 (R/W)	DAQ SW version	31...0	Power-up value: 0
Control register 1	YY08000C (R/W)	Not used	31...0	Power-up value: 0
Status register 1	YY080010 (R)	Not used	31...0	0x00c0ffee
Pulse 1	YY080014 (W)	Not used	-	-
Control register 2	YY080018 (R/W)	Not used	31...0	Power-up value: 0
Control register 3	YY08001C (R/W)	Not used	31...0	Power-up value: 0
Status register 2	YY080020 (R)	Not used	31...0	0x00000cdf

DataIO FPGA 2

Name	Address	Description	Databits	Data
Firmware version	YY0C0000 (R)	Firmware version	31...0	0x0d509190
Reset	YY0C0004 (W)	Reset FPGA	-	-
DAQ SW version	YY0C0008 (R/W)	DAQ SW version	31...0	Power-up value: 0
Control register 1	YY0C000C (R/W)	Not used	31...0	Power-up value: 0
Status register 1	YY0C0010 (R)	Not used	31...0	0x00c0ffee
Pulse 1	YY0C0014 (W)	Not used	-	-
Control register 2	YY0C0018 (R/W)	Not used	31...0	Power-up value: 0
Control register 3	YY0C001C (R/W)	Not used	31...0	Power-up value: 0
Status register 2	YY0C0020 (R)	Not used	31...0	0x00000cdf

Control FPGA

Name	Address	Description	Databits	Data
Firmware version	YY000000 (R)	Firmware version	31...0	0x0c508110
Reset	YY000004 (W)	Reset FPGA	-	-
DAQ SW version	YY000008 (R/W)	DAQ SW version	31...0	Power-up value: 0
Control register 1	YY00000C (R/W)	Bunch Count Shift	7...0	Power-up value: 41
Status register 1	YY000010 (R)	Not used	31...0	0x00c0ffee
Pulse 1	YY000014 (W)	Not used	-	-
Control register 2	YY000018 (R/W)	Not used	31...0	Power-up value: 0
Control register 3	YY00001C (R/W)	Not used	31...0	Power-up value: 0
Status register 2	YY000020 (R)	Not used	31...0	0xdeadbeef
IDPROM	YY100000 – YY10007C (R)	IDPROM	31...24	

IDPROM			
YY100000	0	YY10003C	
YY100004	0	YY100040	X
YY100008	x	YY100044	F
YY10000C	x	YY100048	T
YY100010		YY10004C	
YY100014	1	YY100050	R
YY100018	0	YY100054	X
YY10001C	5	YY100058	
YY100020		YY10005C	
YY100024	P	YY100060	
YY100028	U	YY100064	
YY10002C	L	YY100068	
YY100030	S	YY10006C	
YY100034	A	YY100070	
YY100038	R	YY100074	
		YY100078	
		YY10007C	

DataIO1 DAQ readout

Word count registers

Mezzanine card 1

Channel 1

Buffer 0 XX080800
Buffer 1 XX080900
Buffer 2 XX080A00
Buffer 3 XX080B00

Channel 2

Buffer 0 XX080804
Buffer 1 XX080904
Buffer 2 XX080A04
Buffer 3 XX080B04

Channel 3

Buffer 0 XX080808
Buffer 1 XX080908
Buffer 2 XX080A08
Buffer 3 XX080B08

Mezzanine card 2

Channel 1

Buffer 0 XX08080C
Buffer 1 XX08090C
Buffer 2 XX080A0C
Buffer 3 XX080B0C

Channel 2

Buffer 0 XX080810
Buffer 1 XX080910
Buffer 2 XX080A10
Buffer 3 XX080B10

Channel 3

Buffer 0 XX080814
Buffer 1 XX080914
Buffer 2 XX080A14
Buffer 3 XX080B14

RAM Read VME addresses

Mezzanine card 1

Channel 1

Buffer 0 XX880000-XX8801FC
Buffer 1 XX980000-XX9801FC
Buffer 2 XXA80000-XXA801FC
Buffer 3 XXB80000-XXB801FC

Channel 2

Buffer 0 XX880200-XX883FC
Buffer 1 XX980200-XX9803FC
Buffer 2 XXA80200-XXA803FC
Buffer 3 XXB80200-XXB803FC

Channel 3

Buffer 0 XX880400-XX8805FC
Buffer 1 XX980400-XX9805FC
Buffer 2 XXA80400-XXA805FC
Buffer 3 XXB80400-XXB805FC

Mezzanine card 2

Channel 1

Buffer 0 XX880800-XX88097C
Buffer 1 XX980800-XX98097C
Buffer 2 XXA80800-XXA8097C
Buffer 3 XXB80800-XXB8097C

Channel 2

Buffer 0 XX880A00-XX880BFC
Buffer 1 XX980A00-XX980BFC
Buffer 2 XXA80A00-XXA80BFC
Buffer 3 XXB80A00-XXB80BFC

Channel 3

Buffer 0 XX880C00-XX880DFC
Buffer 1 XX980C00-XX980DFC
Buffer 2 XXA80C00-XXA80DFC
Buffer 3 XXB80C00-XXB80DFC

DataIO2 DAQ readout

Word count registers

Mezzanine card 1

Channel 1

Buffer 0 XX0C0800
Buffer 1 XX0C0900
Buffer 2 XX0C0A00
Buffer 3 XX0C0B00

Channel 2

Buffer 0 XX0C0804
Buffer 1 XX0C0904
Buffer 2 XX0C0A04
Buffer 3 XX0C0B04

Channel 3

Buffer 0 XX0C0808
Buffer 1 XX0C0908
Buffer 2 XX0C0A08
Buffer 3 XX0C0B08

Mezzanine card 2

Channel 1

Buffer 0 XX0C080C
Buffer 1 XX0C090C
Buffer 2 XX0C0A0C
Buffer 3 XX0C0B0C

Channel 2

Buffer 0 XX0C0810
Buffer 1 XX0C0910
Buffer 2 XX0C0A10
Buffer 3 XX0C0B10

Channel 3

Buffer 0 XX0C0814
Buffer 1 XX0C0914
Buffer 2 XX0C0A14
Buffer 3 XX0C0B14

RAM Read VME addresses

Mezzanine card 1

Channel 1

Buffer 0 XX8C0000-XX8C01FC
Buffer 1 XX9C0000-XX9C01FC
Buffer 2 XXAC0000-XXAC01FC
Buffer 3 XXBC0000-XXBC01FC

Channel 2

Buffer 0 XX8C0200-XX8C3FC
Buffer 1 XX9C0200-XX9C3FC
Buffer 2 XXAC0200-XXAC3FC
Buffer 3 XXBC0200-XXBC3FC

Channel 3

Buffer 0 XX8C0400-XX8C5FC
Buffer 1 XX9C0400-XX9C5FC
Buffer 2 XXAC0400-XXAC5FC
Buffer 3 XXBC0400-XXBC5FC

Mezzanine card 2

Channel 1

Buffer 0 XX8C0800-XX8C097C
Buffer 1 XX9C0800-XX9C097C
Buffer 2 XXAC0800-XXAC097C
Buffer 3 XXBC0800-XXBC097C

Channel 2

Buffer 0 XX8C0A00-XX8C0BFC
Buffer 1 XX9C0A00-XX9C0BFC
Buffer 2 XXAC0A00-XXAC0BFC
Buffer 3 XXBC0A00-XXBC0BFC

Channel 3

Buffer 0 XX8C0C00-XX8C0DFC
Buffer 1 XX9C0C00-XX9C0DFC
Buffer 2 XXAC0C00-XXAC0DFC
Buffer 3 XXBC0C00-XXBC0DFC

The following changes have been made:

DataIO FPGAs

-Control Register 1 is now in use.

-Bits 5:0 of Control Register 1 (0x00000C) are used as individual channel-enables:

Bit 0 : Mezz Card 1, Channel 1

Bit 1 : Mezz Card 1, Channel 2

Bit 2 : Mezz Card 1, Channel 3

Bit 3 : Mezz Card 2, Channel 1

Bit 4 : Mezz Card 2, Channel 2

Bit 5 : Mezz Card 2, Channel 3

-A bit value of '1' enables the channel.

Control FPGA

-Control Registers 2 and 3 are now in use, and State Registers 1 and 2 were added.

- Bit 0 of Control Register 2 (0x000018) in the VME Interface determines if the aborts are ignored:

Bit 0 = 0: do not ignore event aborts

Bit 0 = 1: ignore any event aborts

- The power-up value is 1

- Control Register 3 is now used for storing the delay for clearing the word counts in the FILAR_Overflow_Detection, and also for storing the maximum number of words that can be sent before an overflow is triggered:

Bits 19:0 - number of timer ticks to clear a word count (each tick is 12.5 ns)

Bits 29:20 - word count maximum before overflow occurs (should be a little less than 512)

- The power-up value of bits 19:0 is 16, and the power-up value of bits 29:20 is 1023

- State Register 1 (0x000024) is a read-only register that contains the states of some of the signals from the FILAR_Overflow_Detection component:

Bits 31:30 - "00"

Bits 29:20 - word count register 1

Bits 19:10 - word count register 0

Bits 9:0 - current word count

- State Register 2 (0x000028) is a read-only register that contains the states of some of the signals from the FILAR_Overflow_Detection component:

Bits 31:28 - "0000"

Bit 27 - timer 3 enable

Bit 26 - timer 2 enable

Bit 25 - timer 1 enable

Bit 24 - timer 0 enable

Bits 23:22 - event count

Bit 21 - total word count \geq word count max

Bit 20 - overflow bit

Bits 19:10 - word count register 3

Bits 9:0 - word count register 2