/CDF/DOC/TRIGGER/CDFR/8871
November 29, 2007
Version 1.7

Specification for Level 2 TrackList Boards with SLAM Input

Heather Gerberich, Richard Hughes, Ben Kilminster, Kevin Lannon, Ryan Mokos, Kevin Pitts, Greg Veramendi, Peter Wilson, Brian Winer

0. Overview

This is the specification for use of Pulsar boards to replace existing XTRP to SVT and XTRP to L2 path with a higher bandwidth path from the SLAM. The design assumes use of 2 Pulsar boards, each handling data from 12 SLAM boards. Data is sparsified, filtered if desired, and merged into separate lists for SVT and L2. Pulsar B is daisy chained to Pulsar A. The L2 and SVT lists are put together in Pulsar A and forwarded to the L2 Filar and SVT, respectively. Data between the SLAM and Pulsar boards and between the Pulsar boards is sent on standard XFT fibers and received on XFT RX Mezzanine cards. The data to the SVT is sent using the standard SVT cable, and the data to L2 is sent via S-Link from a Pulsar Aux card. The latency from L1A to receipt of last track by L2 FILAR PCI and SVT merger card must be < 10μs for events with 50 tracks. In addition, the Tracklist board generates event abort signals that can be used by other boards to prevent the sending of extra, unwanted data.

There are 3 different firmware versions: two for the control FPGAs on each Pulsar, and one for the 4 Input ("I/O") FPGAs.

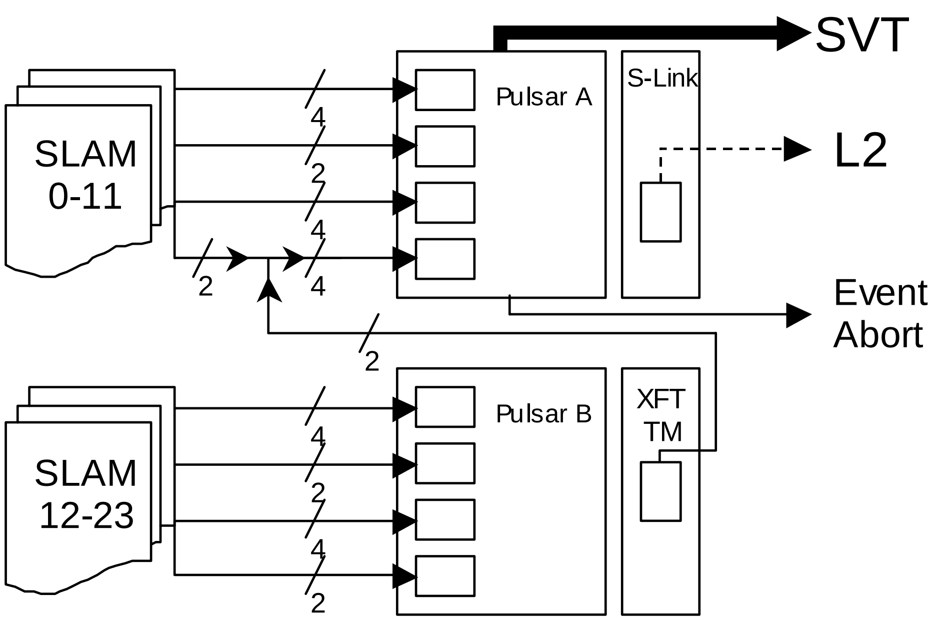

Figure 1: Components and connections of Tracklist upgrade. The figure above shows a daisy-chain configuration.

The Pulsar boards have two jumpers that must be configured differently for Pulsar A and Pulsar B:

- Pulsar A: jumper P3clk1 is set to pins 2 & 3 (bottom pins), and jumper P3clk2 is set to pins 1 & 2 (also bottom pins as the jumper pinouts are reversed).
- Pulsar B: jumper P3clk1 is set to pins 1 & 2 (top pins), and the setting of jumper P3clk2 does not matter.

1. General specs for Pulsar firmware

This section is a summary of the requirements for Pulsar firmware described in the note titled, "Pulsar Firmware for L2 trigger upgrade."

a. Register Space

All VME interface components have three status registers (read only), four control registers (read/write), and two pulse registers (write only). These registers are used differently in different firmware, but the first two registers are reserved. The first status register has a firmware version value in it. The first pulse register is used to reset the FPGA.

DataIO FPGA 1

Name	Address	Type
Firmware version	YY080000	R
Reset	YY080004	W
Control register 1	YY080008	R/W
Control register 2	YY08000C	R/W
Status register 1	YY080010	R
Pulse 1	YY080014	W
Control register 3	YY080018	R/W
Control register 4	YY08001C	R/W
Status register 2	YY080020	R

DataIO FPGA 2

Name	Address	Type
Firmware version	YY0C0000	R
Reset	YY0C0004	W
Control register 1	YY0C0008	R/W
Control register 2	YY0C000C	R/W
Status register 1	YY0C0010	R
Pulse 1	YY0C0014	W
Control register 3	YY0C0018	R/W
Control register 4	YY0C001C	R/W
Status register 2	YY0C0020	R

Control FPGA

Name	Address	Type
Firmware version	YY000000	R
Reset	YY000004	W
Control register 1	YY000008	R/W
Control register 2	YY00000C	R/W
Status register 1	YY000010	R
Pulse 1	YY000014	W
Control register 3	YY000018	R/W
Control register 4	YY00001C	R/W
Status register 2	YY000020	R

YY = VME address bits 31..24, not used by the firmware.

Table 1: VME interface registers

b. DAQ RAMs

Each FPGA has two DAQ RAMs. We have chosen this implementation so that the interface to the DAQ RAMs is identical to all Pulsars and to all FPGAs. However, in some cases, none, or only one of them, is actually used. For example, in the Pulsar SVT board, the DAQ RAMs in the DATAIO FPGAs are always empty. The SVT board only uses the two DAQ RAMs in the Control FPGA.

We have labeled the first DAQ RAM on an FPGA as DAQ RAM 1 and the second as DAQ RAM 2. Each DAQ RAM is divided into four buffers corresponding to the four L2 DAQ buffers. To each buffer a word count register is associated, which tells the number of words in that buffer.

Each buffer can also be divided into subdivisions. For example, one DAQ RAM can have data from eight different inputs. The use of the DAQ RAMs in different firmware is described in more detail later on in this document.

The VME interface component uses the VME address bits to determine which DAQ RAM is being read out and enables that DAQ RAM's output to the VME data bus. Also, the word count registers are enabled to the VME data bus the same way.

When reading out DAQ RAMs, the VME address bit 17 selects between the DAQ RAMs inside one FPGA.

VME address bit 17	**Selected DAQ RAM**
0	DAQ RAM 1
1	DAQ RAM 2

Table 2: VME address bit for DAQ RAM selection

When reading out DAQ RAMs, VME address bit 23 is set high, bit 22 is set low, and bits 20 and 21 select which buffer is read out. This follows CDF speciation for DAQ readout defined in CDF note 2388.

VME address bit				**Selected buffer**
23	**22**	**21**	**20**	
1	0	0	0	Buffer 0
1	0	0	1	Buffer 1
1	0	1	0	Buffer 2
1	0	1	1	Buffer 3

Table 3: VME address bits for DAQ RAM buffer selection

VME addresses for the word count registers are listed in Table 4 below. Some firmware has more than one word count register per DAQ RAM.

DataIO FPGA 1

DAQ RAM	Buffer #	Address
1	0	YY080800
1	1	YY080900
1	2	YY080A00
1	3	YY080B00
2	0	YY080804
2	1	YY080904
2	2	YY080A04
2	3	YY080B04

DataIO FPGA 2

DAQ RAM	Buffer #	Address
1	0	YY0C0800
1	1	YY0C0900
1	2	YY0C0A00
1	3	YY0C0B00
2	0	YY0C0804
2	1	YY0C0904
2	2	YY0C0A04
2	3	YY0C0B04

Control FPGA

DAQ RAM	Buffer #	Address
1	0	YY000800
1	1	YY000900
1	2	YY000A00
1	3	YY000B00
2	0	YY000804
2	1	YY000904
2	2	YY000A04
2	3	YY000B04

YY = VME address bits 31..24, not used by the firmware.

Table 4: Word count register VME addresses

In the beginning of each buffer on the DAQ RAM 1 in the Control FPGA, there is a DAQ Header Word. The format follows CDF note 2388. Currently, Pulsar firmware does not provide Geographical Address in the DAQ Header Word.

Bit	Description
0..7	Bunch Counter Value
8..12	Geographical Address
13..22	Board Serial Number
23..31	Board Type

Table 5: DAQ Header Word format

c. IDPROM

All Control FPGAs have a read-only memory that contains the values of an IDPROM. IDPROM format is also defined in CDF note 2388.

For all Control FPGA firmware, an IDPROM is included in the VME interface. The IDPROM read only memory values are in a memory input file (.mif), which is taken in into compilation when compiling the firmware.

d. Board Type

Each Pulsar board has been assigned its own Board type. The Board type value is put into the IDPROM, DAQ header word, and in the S-LINK data stream as part of a header word. Board type is used to distinguish data from different Pulsar boards in the trigger system.

Board type	**Description**
081	L2 Pulsar Muon/XTRP Rx IIa
083	L2 Pulsar SVT Road Warrior
085	L2 Pulsar Muon/XTRP/L1 Tx or SVT XTRP-emu
086	L2 Pulsar Muon/XTRP/L1 Rx IIb
087	L2 Pulsar SHOWERMAX Tx
088	L2 Pulsar SHOWERMAX Rx
089	L2 Pulsar Cluster/PreFred Tx
090	L2 Pulsar Cluster/PreFred Rx
091	L2 Pulsar SVT Tx
092	L2 Pulsar SVT Rx
093	L2 Pulsar Merger Tx
094	L2 Pulsar Merger Rx
095	L2 Pulsar L2TS Tx
096	L2 Pulsar L2TS
097	L2 Pulsar L1 Scaler
098	L2 Pulsar SVT TF
099	L2 Pulsar test one
100	L2 Pulsar test two
101	L2 Pulsar Stereo Tx
102	L2 Pulsar Stereo Rx
103	SVT Pulsar Hit Buffer
107	Tracklist A
108	Tracklist B

Table 6: Pulsar Board types

2. Firmware for I/O FPGAs

a. Inputs to I/O FPGAs

Each Tracklist I/O FPGA has 8 input channels (4 per mezzanine card). Channels 0-5 are designed to receive SLAM board data, and channels 6 and 7 are designed to receive 32-bit data words (16 bits per channel, which are combined into 32 bit words) in the internal Tracklist data format (see Table 10). The combination of channels 6 and 7 will be referred to as channel 6 for the remainder of this document.

A 16-bit communication protocol is used for the data transfer from the SLAM to the Pulsar mezzanine cards. The data from each SLAM board is packed into one 12-word packet for each event. The SLAM sends every event synchronously to the Tracklist Pulsar and sets data_valid low for abort gaps. The Tracklist Pulsar checks the data and puts it into a pipeline to wait for the L1 accept.

A control bit (bit 15) in each word is reserved to define the first word of the data packet. Otherwise, it is set to 0 for the other 11 data words (see Table 7). The SLAM always sends 12 track data words in ϕ-order, one for each Linker chip, or 1.25^{o}. The data format is identical to the format of the data sent to the XTRP. Bits 12 and 14 are reserve bits. The Tracklist board drops any extra data words sent after the 12 track words.

The I/O FPGA firmware also has the ability to receive 32-bit data from another Pulsar in channels 3 and 4 of the lower mezzanine card (this is channel 6; see Table 10 for the format). This feature is only used for the lower I/O FPGA on Pulsar A. The FPGA concatenates this data to the data it received from the other SLAM boards.

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data T0	1	R1	B0	R	St	pT	pT	pT	pT	pT	pT	pT	S	ϕ	ϕ	ϕ
T1…T11	0	R1	B0	R	St	pT	pT	pT	pT	pT	pT	pT	S	ϕ	ϕ	ϕ

Table 7: Data format for SLAM $\rightarrow$ Pulsar link. The 12 words are all track words. R and R1 are reserved bits, B0 is the bunch count 0 bit, St is the stereo confirmation bit, and S is the short track bit.

b. Functionality and Registers of I/O FPGAs

Each fiber input is associated with a particular Linker chip number. Each fiber input is individually maskable via a masking VME register. Masking allows full operation of the board while ignoring the state of the masked fiber (i.e., unplugged, generating errors, etc).

The I/O FPGA receives the data from each SLAM input. The I/O FPGA performs the following checks and records errors in both the trailer word and a VME-accessible register (see Table 9).

- Check that there are exactly 12 words in each data packet
- Check that the B0 bit in the first track word matches a delayed B0 signal from the backplane

The I/O FPGA sparsifies (removes tracks with $p_T \geq$ 0x60) and appends the SLAM ID (0-23—set by a register for each channel) and Phi index (0-11) to each valid track (see output section for format). This sparsified list is sent to the control FPGA for concatenation and filtering (see output).

There are readout buffers in each I/O FPGA that store the unsparsified data coming in on the fibers from the SLAM boards. The data is stored in the L2 buffer seen on the backplane. There is also a circular L2 buffer (which is a buffer to which valid data is continuously written in a looping fashion, with a pointer specifying the last address to which a word was written) containing the sparcified, concatenated data packets immediately before they are merged into one packet and sent to the control FPGA.

The following registers are VME-accessible:

- One register for each input containing error bits for any errors found when doing checks. Error bits are stored until they are cleared by a VME-write to the same register, HRR, channel reset, or FPGA reset.
- A set of registers for reading out the L2 buffers and the circular L2 buffer
- A register to define which fiber inputs are active
- A register for each SLAM channel to define the data packet length (defaults to 12)
- Two sets of registers that contain the number of words in the DAQ buffers for each L2 buffer: one set for channels 0-5 and one set for channel 6. The registers for channels 0-5 all contain the value 96, and the registers for channel 6 are dynamically set to the number of data words ("# of data words in packet" from the trailer word) plus 2.
- A set of registers to define the SLAM ID for each SLAM input channel
- A register to define the L1 pipeline delay
- A register to define the delay for the B0 signal
- An input data mask register to mask out arbitrary data bits

Global Register	I/O FPGA 1 Address	I/O FPGA 2 Address	R/W	Notes
Firmware Version	xx080000	xx0C0000	R	---
FPGA-Wide Reset	xx080004	xx0C0004	W	Just write once (generates a pulse)
Bunch Counter Offset	xx08000C	xx0C000C	R/W	Only bits 7:0; in CDFCLK cycles; default = 41
Status Register 1	xx080010	xx0C0010	R	0x00C0FFEE
Status Register 2	xx080020	xx0C0020	R	0x00000CDF
Errors in Channels 0 and 1	xx080030	xx0C0030	R/W	Write anything to clear
Errors in Channels 2 and 3	xx080034	xx0C0034	R/W	Write anything to clear
Errors in Channels 4 and 5	xx080038	xx0C0038	R/W	Write anything to clear
Errors in Channel 6	xx08003C	xx0C003C	R/W	Write anything to clear
Active Channels	xx080040	xx0C0040	R/W	Only bits 6:0; 1 bit per channel; reset FPGA after changing
B0 Offset (Number of Events)	xx080044	xx0C0044	R/W	Only bits 5:0; in BCs (events)
Debug Signal Selector	xx080048	xx0C0048	R/W	Only bits 3:0
Input Data Mask	xx08004C	xx0C004C	R/W	Only bits 15:0; default = 0xFFF7
L2 Circular Buffer Address	xx080050	xx0C0050	R	Only bits 7:0
L2 Circular Buffer (Merged Data)	xx8A1000 - xx8A13FC	xx8E1000 - xx8E13FC	R	256 words deep
Ch 0-5 Buf 0 Word Count	xx080800	xx0C0800	R	= 96
Ch 0-5 Buf 1 Word Count	xx080900	xx0C0900	R	= 96
Ch 0-5 Buf 2 Word Count	xx080A00	xx0C0A00	R	= 96
Ch 0-5 Buf 3 Word Count	xx080B00	xx0C0B00	R	= 96
Ch 6 Buf 0 Word Count	xx080804	xx0C0804	R	= Actual packet length (initially = 2) (total # of words, not just data words)
Ch 6 Buf 1 Word Count	xx080904	xx0C0904	R	= Actual packet length (initially = 2) (total # of words, not just data words)
Ch 6 Buf 2 Word Count	xx080A04	xx0C0A04	R	= Actual packet length (initially = 2) (total # of words, not just data words)
Ch 6 Buf 3 Word Count	xx080B04	xx0C0B04	R	= Actual packet length (initially = 2) (total # of words, not just data words)

Channel 0 Register	I/O FPGA 1 Address	I/O FPGA 2 Address	R/W	Notes
Reset	xx000100	xx000100	W	Just write once (generates a pulse)
Data Packet Length	xx000200	xx000200	R/W	Only bits 4:0; default = 12
SLAM ID	xx000300	xx000300	R/W	Only bits 4:0
L2 Buffer 0 (Unsparsified Data)	xx800000 - xx80003C	xx800000 - xx80003C	R	Only read first 16 words; # data words in packet not included
L2 Buffer 1 (Unsparsified Data)	xx900000 - xx90003C	xx900000 - xx90003C	R	Only read first 16 words; # data words in packet not included
L2 Buffer 2 (Unsparsified Data)	xxA00000 - xxA0003C	xxA00000 - xxA0003C	R	Only read first 16 words; # data words in packet not included
L2 Buffer 3 (Unsparsified Data)	xxB00000 - xxB0003C	xxB00000 - xxB0003C	R	Only read first 16 words; # data words in packet not included

Channel 1 Register	I/O FPGA 1 Address	I/O FPGA 2 Address	R/W	Notes
Reset	xx000104	xx000104	W	Just write once (generates a pulse)
Data Packet Length	xx000204	xx000204	R/W	Only bits 4:0; default = 12
SLAM ID	xx000304	xx000304	R/W	Only bits 4:0
L2 Buffer 0 (Unsparsified Data)	xx800040 - xx80007C	xx800040 - xx80007C	R	Only read first 16 words; # data words in packet not included
L2 Buffer 1 (Unsparsified Data)	xx900040 - xx90007C	xx900040 - xx90007C	R	Only read first 16 words; # data words in packet not included
L2 Buffer 2 (Unsparsified Data)	xxA00040 - xxA0007C	xxA00040 - xxA0007C	R	Only read first 16 words; # data words in packet not included
L2 Buffer 3 (Unsparsified Data)	xxB00040 - xxB0007C	xxB00040 - xxB0007C	R	Only read first 16 words; # data words in packet not included

Channel 2 Register	I/O FPGA 1 Address	I/O FPGA 2 Address	R/W	Notes
Reset	xx000108	xx000108	W	Just write once (generates a pulse)
Data Packet Length	xx000208	xx000208	R/W	Only bits 4:0; default = 12
SLAM ID	xx000308	xx000308	R/W	Only bits 4:0
L2 Buffer 0 (Unsparsified Data)	xx800080 - xx8000BC	xx800080 - xx8000BC	R	Only read first 16 words; # data words in packet not included
L2 Buffer 1 (Unsparsified Data)	xx900080 - xx9000BC	xx900080 - xx9000BC	R	Only read first 16 words; # data words in packet not included
L2 Buffer 2 (Unsparsified Data)	xxA00080 - xxA000BC	xxA00080 - xxA000BC	R	Only read first 16 words; # data words in packet not included
L2 Buffer 3 (Unsparsified Data)	xxB00080 - xxB000BC	xxB00080 - xxB000BC	R	Only read first 16 words; # data words in packet not included
Channel 3 Register	**I/O FPGA 1 Address**	**I/O FPGA 2 Address**	**R/W**	**Notes**
Reset	xx00010C	xx00010C	W	Just write once (generates a pulse)
Data Packet Length	xx00020C	xx00020C	R/W	Only bits 4:0; default = 12
SLAM ID	xx00030C	xx00030C	R/W	Only bits 4:0
L2 Buffer 0 (Unsparsified Data)	xx8000C0 - xx8000FC	xx8000C0 - xx8000FC	R	Only read first 16 words; # data words in packet not included
L2 Buffer 1 (Unsparsified Data)	xx9000C0 - xx9000FC	xx9000C0 - xx9000FC	R	Only read first 16 words; # data words in packet not included
L2 Buffer 2 (Unsparsified Data)	xxA000C0 - xxA000FC	xxA000C0 - xxA000FC	R	Only read first 16 words; # data words in packet not included
L2 Buffer 3 (Unsparsified Data)	xxB000C0 - xxB000FC	xxB000C0 - xxB000FC	R	Only read first 16 words; # data words in packet not included
Channel 4 Register	**I/O FPGA 1 Address**	**I/O FPGA 2 Address**	**R/W**	**Notes**
Reset	xx000110	xx000110	W	Just write once (generates a pulse)
Data Packet Length	xx000210	xx000210	R/W	Only bits 4:0; default = 12
SLAM ID	xx000310	xx000310	R/W	Only bits 4:0
L2 Buffer 0 (Unsparsified Data)	xx800100 - xx80013C	xx800100 - xx80013C	R	Only read first 16 words; # data words in packet not included
L2 Buffer 1 (Unsparsified Data)	xx900100 - xx90013C	xx900100 - xx90013C	R	Only read first 16 words; # data words in packet not included
L2 Buffer 2 (Unsparsified Data)	xxA00100 - xxA0013C	xxA00100 - xxA0013C	R	Only read first 16 words; # data words in packet not included
L2 Buffer 3 (Unsparsified Data)	xxB00100 - xxB0013C	xxB00100 - xxB0013C	R	Only read first 16 words; # data words in packet not included
Channel 5 Register	**I/O FPGA 1 Address**	**I/O FPGA 2 Address**	**R/W**	**Notes**
Reset	xx000114	xx000114	W	Just write once (generates a pulse)
Data Packet Length	xx000214	xx000214	R/W	Only bits 4:0; default = 12
SLAM ID	xx000314	xx000314	R/W	Only bits 4:0
L2 Buffer 0 (Unsparsified Data)	xx800140 - xx80017C	xx800140 - xx80017C	R	Only read first 16 words; # data words in packet not included
L2 Buffer 1 (Unsparsified Data)	xx900140 - xx90017C	xx900140 - xx90017C	R	Only read first 16 words; # data words in packet not included
L2 Buffer 2 (Unsparsified Data)	xxA00140 - xxA0017C	xxA00140 - xxA0017C	R	Only read first 16 words; # data words in packet not included
L2 Buffer 3 (Unsparsified Data)	xxB00140 - xxB0017C	xxB00140 - xxB0017C	R	Only read first 16 words; # data words in packet not included
Channel 6 Register	**I/O FPGA 1 Address**	**I/O FPGA 2 Address**	**R/W**	**Notes**
Reset	xx000118	xx000118	W	Just write once (generates a pulse)
L2 Buffer 0 (Pulsar Data)	xx820000 - xx8203FC	xx820000 - xx8203FC	R	256 words deep
L2 Buffer 1 (Pulsar Data)	xx920000 - xx9203FC	xx920000 - xx9203FC	R	256 words deep
L2 Buffer 2 (Pulsar Data)	xxA20000 - xxA203FC	xxA20000 - xxA203FC	R	256 words deep
L2 Buffer 3 (Pulsar Data)	xxB20000 - xxB203FC	xxB20000 - xxB203FC	R	256 words deep

Table 8: Tracklist I/O FPGA register space summary.

Bit for Channel X	Bit for Channel X+1	Error
Bit 0	Bit 16	Words in Packet
Bit 1	Bit 17	L1 B0 Bit Error
Bit 2	Bit 18	L1 Word Count Error

Table 9: Tracklist I/O FPGA error flags register definition.

c. Outputs of I/O FPGAs

There is a 32-bit connection between each I/O FPGA and the control FPGA. The format of the data is shown in Table 10.

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Header	1	0	Not used				L2 Buff		Not used					Turn #		
Data 0	0	R1	B0	R	St	pT	pT	pT	pT	pT	pT	pT	S	ϕ	ϕ	ϕ
…	...															
Data N	0	R1	B0	R	St	pT	pT	pT	pT	pT	pT	pT	S	ϕ	ϕ	ϕ
Trailer	1	1	Error flags						Bunch Counter							

bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Header	1	0	Not used												L2 Buff	
Data 0	0	Not used						Phi index				SLAM ID				
…	...															
Data N	0	Not used						Phi index				SLAM ID				
Trailer	1	1	Error flags					# of data words in packet								

Table 10: Internal Tracklist data format for the 32-bit communication between FPGAs and in the daisy-chain connection between the Pulsars.

Bits 0-15 follow the definition of the data sent from the SLAM (see Table 7). Bits 30-31 are the control bits and are defined in the same way as bits 14 and 15. Bits 16-17 of the header word contain the L2 buffer number, and bits 18-29 are not used. The number of data words in the data packet (not including the header and trailer words) is recorded in the trailer word in bits 16-24. The error bits generated by the Pulsar firmware are stored in bits 25-29 and 8-13 in the trailer word (see Table 11). The SLAM ID (0-23) and Phi index (word number 0-11) are stored in the data words in bits 16-20 and 21-24, respectively. Bits 25-30 of the data words are not used.

Bit	Source FPGA	Error
Bit 8	DataIO	Packet Length | L1 Word Count | L1 B0 Bit Error
Bit 9	Control B	L2 Buffer Number Mismatch Error
Bit 10	Control B	Turn Number Mismatch Error
Bit 11	Control B	Bunch Count Mismatch Error
Bit 12	Control B	Packet 1 Length Error
Bit 13	Control B	Packet 2 Length Error
Bit 25	Control A	L2 Buffer Number Mismatch Error
Bit 26	Control A	Turn Number Mismatch Error
Bit 27	Control A	Bunch Count Mismatch Error
Bit 28	Control A	Packet 1 Length Error
Bit 29	Control A	Packet 2 Length Error

Table 11: Tracklist error flags in the trailer word.

3. Firmware for Control FPGA on Pulsar B

a. Inputs to Control FPGA B

The control FPGA on Pulsar B receives the data from the two I/O FPGAs. The data format is described in Table 10.

b. Functionality and Registers of Control FPGA B

The control FPGA B firmware concatenates the data from the two I/O FPGAs, ORs the error bits, and updates the "Number of Words" in the trailer word. The merged data from the I/O FPGAs is stored in a circular L2 buffer (which is a buffer to which valid data is continuously written in a looping fashion, with a pointer specifying the last address to which a word was written). There is also a standard set of L2 buffers to capture the data sent out of Tracklist B.

The firmware performs the following checks and records errors in both the trailer word and a VME accessible register (see Table 13).

- Check the number of data words received from each I/O FPGA with the number of data words specified in each trailer word
- Check that the bunch count and L2 buffer number agree between the two I/O FPGAs

The following registers are VME-accessible:

- One register containing the ORed error bits sent by the I/O FPGAs and any errors found when doing checks. Error bits are stored until they are cleared by a VME-write to the same register, HRR, channel reset, or FPGA reset.
- A set of registers for reading out the L2 buffers and the circular L2 buffer
- A set of registers for the IDPROM

Global Register	Address	R/W	Notes
Firmware Version	xx000000	R	---
FPGA-Wide Reset	xx000004	W	Just write once (generates a pulse)
Status Register 1	xx000010	R	0x00C0FFEE
Status Register 2	xx000020	R	0x00000CDF
Error Flags	xx000030	R/W	Only bits 5:0; Write anything to clear
L2 Circular Buffer Address	xx000050	R	Only bits 8:0
L2 Circular Buffer (Merged Data)	xx820000 - xx8207FC	R	512 words deep
TB Interface Buffer 0 Word Count	xx000800	R	---
TB Interface Buffer 1 Word Count	xx000900	R	---
TB Interface Buffer 2 Word Count	xx000A00	R	---
TB Interface Buffer 3 Word Count	xx000B00	R	---
TB Interface DAQ RAM Buffer 0	xx800000 - xx8003FC	R	256 words deep
TB Interface DAQ RAM Buffer 1	xx900000 - xx9003FC	R	256 words deep
TB Interface DAQ RAM Buffer 2	xxA00000 - xxA003FC	R	256 words deep
TB Interface DAQ RAM Buffer 3	xxB00000 - xxB003FC	R	256 words deep

ID PROM	Address	R/W	Character	ASCII Value
Location 0	xx100000	R	0	0x30000000
Location 1	xx100004	R	0	0x30000000
Location 2	xx100008	R	x	0x78000000
Location 3	xx10000C	R	x	0x78000000
Location 4	xx100010	R		0x20000000
Location 5	xx100014	R	1	0x31000000
Location 6	xx100018	R	0	0x30000000
Location 7	xx10001C	R	8	0x38000000
Location 8	xx100020	R		0x20000000
Location 9	xx100024	R	P	0x50000000
Location 10	xx100028	R	U	0x55000000
Location 11	xx10002C	R	L	0x4C000000
Location 12	xx100030	R	S	0x53000000
Location 13	xx100034	R	A	0x41000000
Location 14	xx100038	R	R	0x52000000
Location 15	xx10003C	R		0x20000000
Location 16	xx100040	R	T	0x54000000
Location 17	xx100044	R	R	0x52000000
Location 18	xx100048	R	A	0x41000000
Location 19	xx10004C	R	C	0x43000000
Location 20	xx100050	R	K	0x4B000000
Location 21	xx100054	R	L	0x4C000000
Location 22	xx100058	R	I	0x49000000
Location 23	xx10005C	R	S	0x53000000
Location 24	xx100060	R	T	0x54000000
Location 25	xx100064	R		0x20000000
Location 26	xx100068	R	B	0x42000000
Location 27	xx10006C	R		0x20000000
Location 28	xx100070	R		0x20000000
Location 29	xx100074	R		0x20000000
Location 30	xx100078	R		0x20000000
Location 31	xx10007C	R		0x20000000

Table 12: Tracklist Control B register space summary.

Bit	Source FPGA	Error
Bit 0	DataIO	Packet Length | L1 Word Count | L1 B0 Bit Error
Bit 1	Control B	L2 Buffer Number Mismatch Error
Bit 2	Control B	Turn Number Mismatch Error
Bit 3	Control B	Bunch Count Mismatch Error
Bit 4	Control B	Packet 1 Length Error
Bit 5	Control B	Packet 2 Length Error

Table 13: Tracklist Control B error flags register definition.

c. Outputs of Control FPGA B

The merged data is sent out the P3 connecter to a Pulsar transition board with an XFT-fiber mezzanine card. The format of the data is described in Table 10.

4. Firmware for Control FPGA on Pulsar A

a. Inputs to Control FPGA A

The control FPGA on Pulsar A receives data from the two I/O FPGAs on Pulsar A in the format described in Table 10.

Control FPGA A also receives the L1 trigger bits on two cables through the front panel of the Pulsar board. Each cable carries 32 bits and a data strobe signal.

b. Functionality and Registers of Control FPGA A

The control FPGA A firmware concatenates the data from the two I/O FPGAs, and performs the same checks on the data as the firmware in Section 3 (Control FPGA on Pulsar B). Duplicate tracks are then removed from the list. Duplicate tracks are defined as tracks with adjacent SLAM numbers and phi index, and where the mini-phi (ϕ) values are less than three apart. Table 14 contains the possibilities (note that the tracks will be adjacent in the list, except for the first and last tracks).

Track 1			**Track 2**		
SLAM #	**phi index**	**ϕ**	**SLAM #**	**Phi index**	**ϕ**
N	5	6	N+1	6	0
N	5	7	N+1	6	0
N	5	7	N+1	6	1
N	11	6	N+1	0	0
N	11	7	N+1	0	0
N	11	7	N+1	0	1

Table 14: The definition of duplicate tracks removed from the list. The track with the lower SLAM # is removed. Track #287 is considered to be low with respect to track #0.

After duplicate removal, the tracks are converted from the internal Tracklist format to the L2 format (see Table 20). Finally, this list is sent along two parallel paths: SVT, which is filtered; and L2, which is not filtered. Filtering of the SVT track list is provided to minimize the number of tracks that need to be handled by the downstream components.

Filtering is accomplished using two registers, which are loaded during configuration. One turns on filtering, and the other is used to store a 64-bit L1 trigger bit mask. The L1 trigger bits for an event are logically ANDed with the L1 trigger bit mask, and the resultant 64 bits are all ORed together. The result is used to choose between the Unfiltered List and the Intermediate List.

List criteria:

- Unfiltered List: all tracks
- Intermediate List: $8 \leq pT \leq 87$, stereo bit value doesn't matter

Three sets of L2 buffers store the track list at different points. A circular L2 buffer is used to store the merged list received from the I/O FPGAs. One set of standard L2 buffers stores the SVT filtered list, and the other set of standard L2 buffers stores the L2 list that is transmitted over the SLINK connection.

In addition, the Control A firmware contains extra L1 trigger bit masks that are used in the same manner just described (except that the result is inverted, meaning the bit masks are enable masks rather than abort masks) to generate event abort signals that are sent to the XFT Pulsar boards via an LVDS cable connected to the TS_Out connector. These abort signals are also broadcast over the backplane via the P2 connector so that any XFT boards in the same crate have access without requiring a cable. These signals are used by the XFT boards to speed up system performance by preventing the transfer of undesired data.

The following registers are VME-accessible:

- One register containing the ORed error bits sent by the I/O FPGAs and any errors found when doing checks. Error bits are stored until they are cleared by a VME-write to the same register, HRR, channel reset, or FPGA reset.
- A set of registers for reading out the L2 buffers and the circular L2 buffer
- A register to define the delay for the B0 signal
- A register for filter settings
- Two registers for the L1 trigger bit mask
- A set of registers for the abort bit masks (actually, enable bit masks)
- A set of registers for reading out the captured L1 trigger bits
- A register that specifies whether the captured L1 trigger bits are inserted into the SLINK data stream
- A set of registers for the IDPROM

Global Register	Address	R/W	Notes
Firmware Version	xx000000	R	---
FPGA-Wide Reset	xx000004	W	Just write once (generates a pulse)
Bunch Count Shift	xx00000C	R/W	Only bits 7:0; in CDFCLK cycles; default = 0
Status Register 1	xx000010	R	0x00C0FFEE
Status Register 2	xx000020	R	0x00000CDF
Error Flags	xx000030	R/W	Only bits 10:0; Write anything to clear
L2 Circular Buffer Address	xx000050	R	Only bits 8:0
Filter Settings	xx000060	R/W	Only bit 0
Low L1 Trigger Bit Mask	xx000070	R/W	Bits 31:0 of the Trigger Bit Mask
High L1 Trigger Bit Mask	xx000074	R/W	Bits 63:32 of the Trigger Bit Mask
Low XFT Abort Bit Mask	xx000080	R/W	Bits 31:0 of the XFT Abort Bit Mask
High XFT Abort Bit Mask	xx000084	R/W	Bits 63:32 of the XFT Abort Bit Mask
Low Cal Abort Bit Mask	xx000090	R/W	Bits 31:0 of the Cal Abort Bit Mask
High Cal Abort Bit Mask	xx000094	R/W	Bits 63:32 of the Cal Abort Bit Mask
Insert L1 Trigger Bits	xx000100	R/W	Only bit 0; default = 1 (insert)
Buffer 0 L1 Trigger Bits	xx000400 - xx000404	R	Trigger bits 63:32 in 0x4; 31:0 in 0x0
Buffer 1 L1 Trigger Bits	xx000410 - xx000414	R	Trigger bits 63:32 in 0x4; 31:0 in 0x0
Buffer 2 L1 Trigger Bits	xx000420 - xx000424	R	Trigger bits 63:32 in 0x4; 31:0 in 0x0
Buffer 3 L1 Trigger Bits	xx000430 - xx000434	R	Trigger bits 63:32 in 0x4; 31:0 in 0x0
L2 Circular Buffer (Merged Data)	xx820000 - xx8207FC	R	512 words deep
SVT Filtered List L2 Buffer 0	xx830000 - xx8301FC	R	128 words deep
SVT Filtered List L2 Buffer 1	xx930000 - xx9301FC	R	128 words deep
SVT Filtered List L2 Buffer 2	xxA30000 - xxA301FC	R	128 words deep
SVT Filtered List L2 Buffer 3	xxB30000 - xxB301FC	R	128 words deep
SLINK Buffer 0 Word Count	xx000800	R	---
SLINK Buffer 1 Word Count	xx000900	R	---
SLINK Buffer 2 Word Count	xx000A00	R	---
SLINK Buffer 3 Word Count	xx000B00	R	---
SLINK DAQ RAM Buffer 0	xx800000 - xx81FFFC	R	---
SLINK DAQ RAM Buffer 1	xx900000 - xx91FFFC	R	---
SLINK DAQ RAM Buffer 2	xxA00000 - xxA1FFFC	R	---
SLINK DAQ RAM Buffer 3	xxB00000 - xxB1FFFC	R	---

ID PROM	Address	R/W	Character	ASCII Value
Location 0	xx100000	R	0	0x30000000
Location 1	xx100004	R	0	0x30000000
Location 2	xx100008	R	x	0x78000000
Location 3	xx10000C	R	x	0x78000000
Location 4	xx100010	R		0x20000000
Location 5	xx100014	R	1	0x31000000
Location 6	xx100018	R	0	0x30000000
Location 7	xx10001C	R	7	0x37000000
Location 8	xx100020	R		0x20000000
Location 9	xx100024	R	P	0x50000000
Location 10	xx100028	R	U	0x55000000
Location 11	xx10002C	R	L	0x4C000000
Location 12	xx100030	R	S	0x53000000
Location 13	xx100034	R	A	0x41000000
Location 14	xx100038	R	R	0x52000000
Location 15	xx10003C	R		0x20000000
Location 16	xx100040	R	T	0x54000000
Location 17	xx100044	R	R	0x52000000
Location 18	xx100048	R	A	0x41000000
Location 19	xx10004C	R	C	0x43000000
Location 20	xx100050	R	K	0x4B000000
Location 21	xx100054	R	L	0x4C000000
Location 22	xx100058	R	I	0x49000000
Location 23	xx10005C	R	S	0x53000000

ID PROM	Address	R/W	Character	ASCII Value
Location 24	xx100060	R	T	0x54000000
Location 25	xx100064	R		0x20000000
Location 26	xx100068	R	A	0x41000000
Location 27	xx10006C	R		0x20000000
Location 28	xx100070	R		0x20000000
Location 29	xx100074	R		0x20000000
Location 30	xx100078	R		0x20000000
Location 31	xx10007C	R		0x20000000

Table 15: Tracklist Control A register space summary.

Bit	Source FPGA	Error
Bit 0	DataIO	Packet Length | L1 Word Count | L1 B0 Bit Error
Bit 1	Control B	L2 Buffer Number Mismatch Error
Bit 2	Control B	Turn Number Mismatch Error
Bit 3	Control B	Bunch Count Mismatch Error
Bit 4	Control B	Packet 1 Length Error
Bit 5	Control B	Packet 2 Length Error
Bit 6	Control A	L2 Buffer Number Mismatch Error
Bit 7	Control A	Turn Number Mismatch Error
Bit 8	Control A	Bunch Count Mismatch Error
Bit 9	Control A	Packet 1 Length Error
Bit 10	Control A	Packet 2 Length Error

Table 16: Tracklist Control A error flags register definition.

Bit	Function
Bit 0	0: SVT Filtering Off; 1: SVT Filtering On

Table 17: Tracklist Control A filter settings register definition.

c. Outputs of Control FPGA A

L2 Output

The L2 Output will be sent out the P3 connector to a Pulsar transition (aux) board, which will send out the data through an S-Link (HOLA) mezzanine card. The data follows the format used in the Pulsar Muon Board, which is defined in CDF note 4152, section 31.14.1 “Pulsar Summary Data.” The relevant parts are repeated here with some modifications for the Tracklist design.

The structure of the data is as follows:

DAQ Header Word
SLINK BOF
SLINK Header 1
SLINK Header 2
Tracklist Header Word
Track 1 Data
…
Track N Data
Tracklist Trailer Word
L1 Trigger bits (bits 0 to 31) (Optional)
L1 Trigger bits (bits 32 to 63) (Optional)
SLINK Trailer
SLINK EOF

Table 18: Structure of Pulsar Tracklist board data sent to L2 via SLINK. The DAQ header word and various SLINK control word definitions are given in Table 19. The bit assignments for the track data are given in Table 20. Insertion of the L1 trigger bits can be enabled/disabled with register 0x000100.

Data Word	**Bit Definition**
DAQ Header Word	Board Type (31:23), Serial Number (22:13), Reserved (12:8), Bunch Counter (7:0)
SLINK BOF	SLINK Beginning of Fragment Control Word (0xB0F00000)
SLINK Header 1	Format (31:24), Source (23:20), Region ID (19:18), Reserved (17:10), Bunch Counter (9:2), L2 Buffer Number (1:0)
SLINK Header 2	Reserved (31:16), Latency (15:0)
SLINK Trailer	Data Size (31:16), Error Flags (15:0)
SLINK EOF	SLINK End of Fragment Control Word (0xE0F00000)

Table 19: Header word and SLINK control word definitions for the Pulsar Tracklist board.

Bit	**Definition**
11:0	Track ϕ
18:12	Track Curvature Bin (pT)
19	Stereo Confirmation (St)
20	Short Track Bit (“S”)
21	End of Packet Bit (Set to 0)
22	End of Event Bit (Set to 0)
31:23	Not Used

Table 20: Bit assignments for L2 and SLAM track data in the Pulsar Tracklist Board. Track ϕ is a combination of mini-ϕ, ϕ-index, and SLAM ID (12 x SLAM ID + ϕ-index, then append mini-ϕ).

Bit	Definition
7:0	Bunch Count
18:8	Reserved for Error Flags (Not Currently Used)
20:19	Level-2 Buffer Number
21	End of Packet (EP) Bit = 1
22	End of Event (EE) Bit = 1
31:23	Not Used

Table 21: Bit assignments for End of Event Word in the Pulsar Tracklist Board.

Bit	Definition
0	XFT Abort
1	Extra Abort
15:2	All 0s

Table 22: Bit assignments for Error Flags in the SLINK Trailer word.

SVT Output

SVT output is on standard SVT cable, and uses the SVT protocol in CDF note 4578.

Event Abort Output

The Control A firmware contains two L1 trigger bit masks for generating event abort signals that can be sent to XFT Pulsar boards (or any other board that could use it) to prevent the transmission of data from unwanted events. One mask is used to create three identical abort signals, and the other mask is used to create a single, separate abort signal. Each abort signal is accompanied by a strobe, which is valid for 25 ns, that is sent 25 ns after the abort signal is valid. Four pairs of signals are sent over an LVDS cable that is connected to the TS_Out connector on the Pulsar board (see Table 23 for the connector pinout), and one pair is sent to the backplane via the P2 connector.

The abort signals are generated as follows: the L1 trigger bits for an event are logically ANDed with the bit mask, the resultant 64 bits are all ORed together, and the final signal is inverted. This means that the masks are effectively enable masks (not abort masks).

Signal	TS_Out Connector Pins
Extra Abort	35 & 36
Extra Strobe	37 & 38
XFT Abort 1	39 & 40
XFT Strobe 1	41 & 42
XFT Abort 2	43 & 44
XFT Strobe 2	45 & 46
XFT Abort 3	49 & 50
XFT Strobe 3	51 & 52

Table 23: Event abort signal pinout on the Pulsar board TS_Out connector.