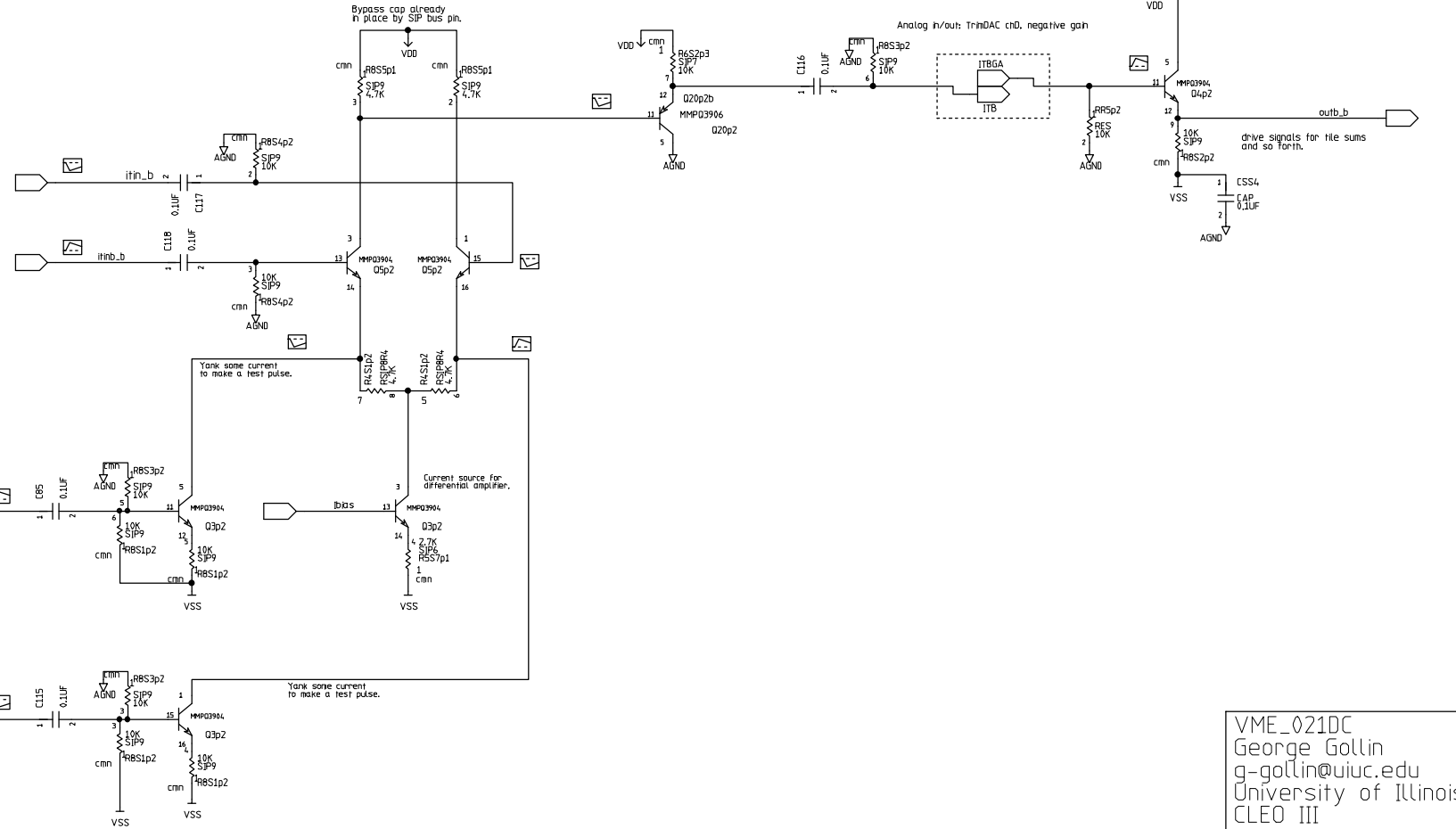
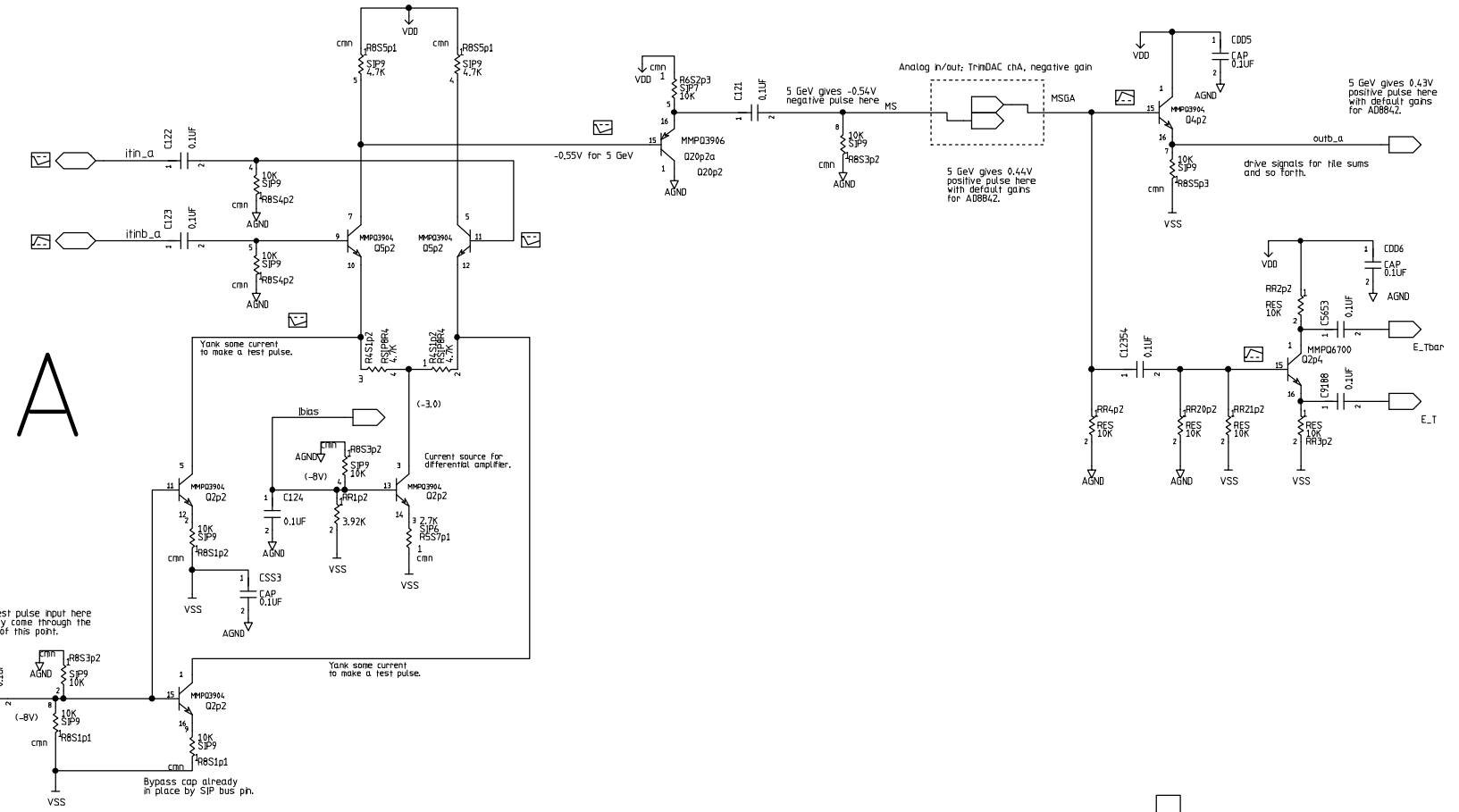


Make a gain-adjusted copy of the mixer/shaper signal;
feed this to tile sum and E_T sum circuitry.

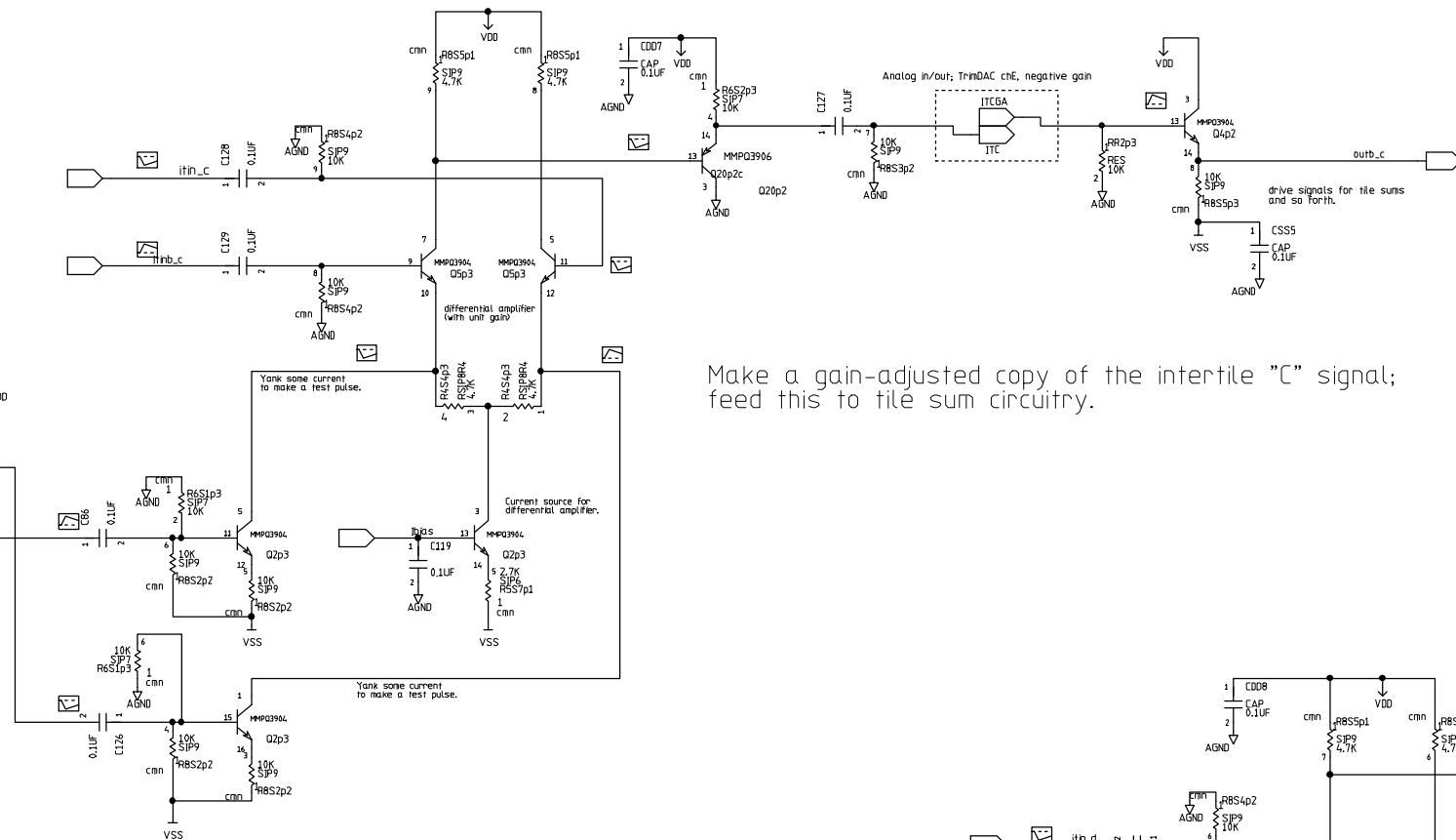
A +/- 56V differential signal
here corresponds to 5 GeV.
Propagation time through the
circuit is about 4ns; less
than for a pulse which enters
the inputs from the mixer/shapers
at the same time as an intertile
pulse.



Make a gain-adjusted copy of the intertile "B" signal;
feed this to tile sum circuitry.

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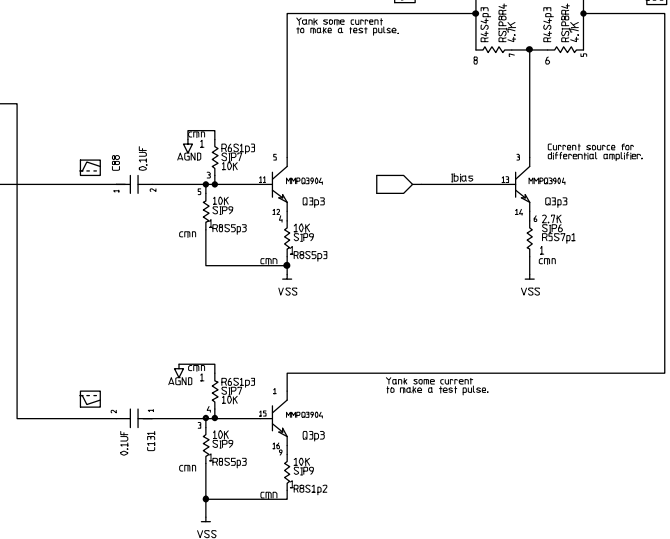
testHCGA
TrinDAC chF



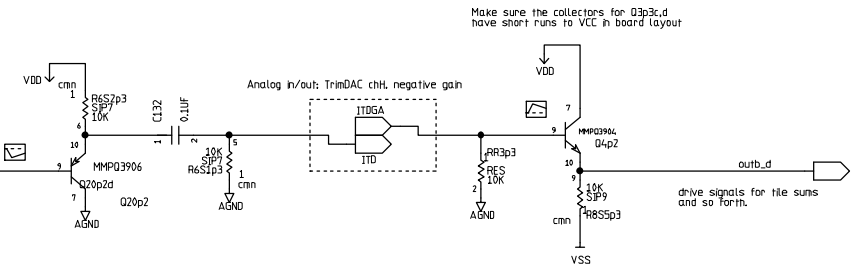
Make a gain-adjusted copy of the intertile "C" signal;
feed this to tile sum circuitry.



testHCGA
TrinDAC chG

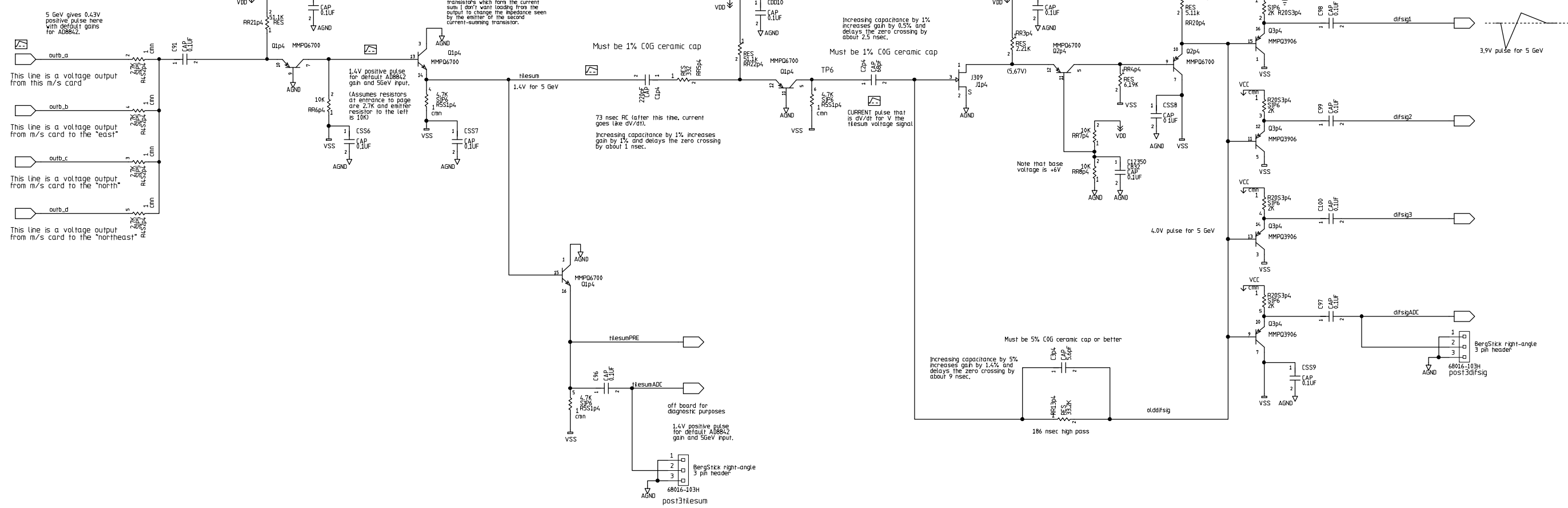


Make a gain-adjusted copy of the intertile "D" signal;
feed this to tile sum circuitry.



Make sure the collectors for 03p3,d
have short runs to VCC n board layout

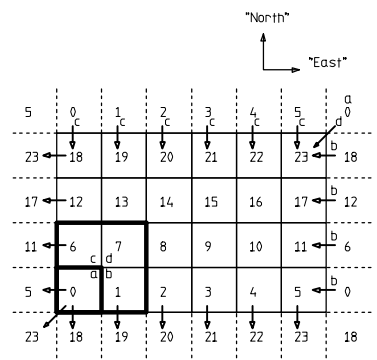
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24 mixer/shaper cards per tiling card.
Indicated: signal export/import across tiling card boundaries.

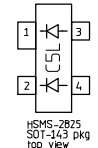
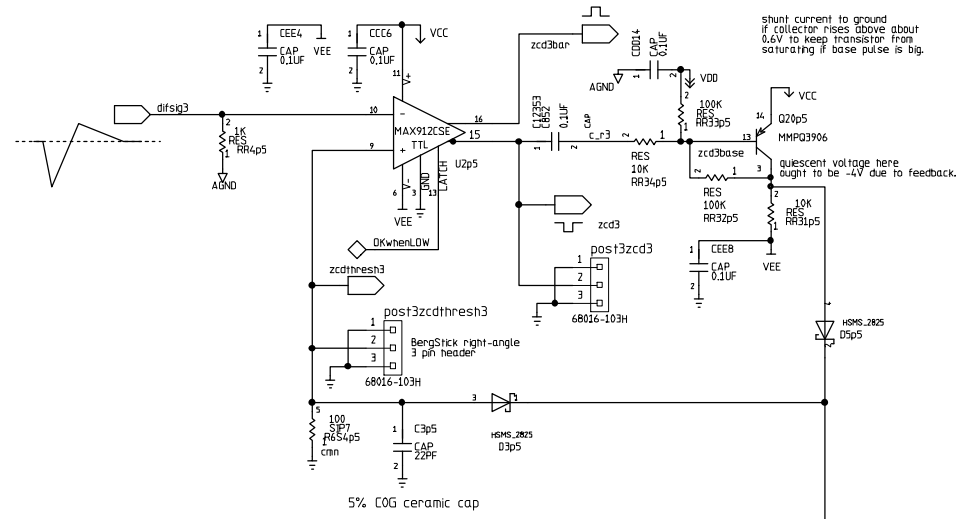
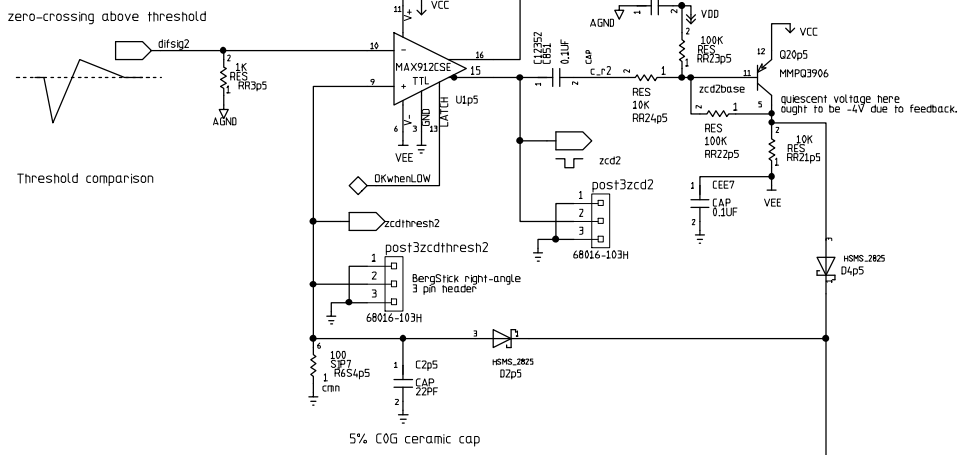
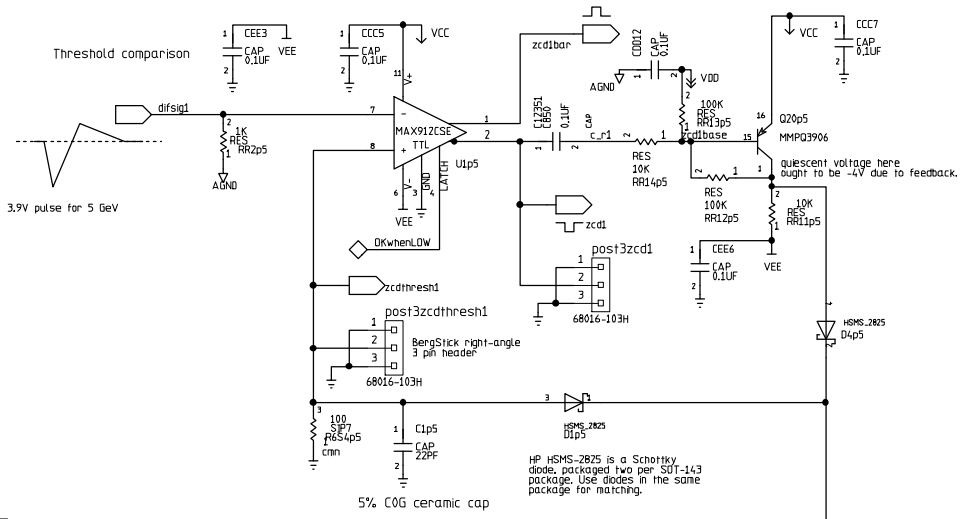
The file rooted in m/s card 0 receives inputs from the following m/s cards:
a input from m/s 0,
b input from m/s 1,
c input from m/s 6,
d input from m/s 7.

The file rooted in m/s card 23 receives inputs from the following m/s cards:
c input from m/s 5 in the "one-to-the-north" tiling card,
d input from m/s 0 in the "one-to-the-northeast" tiling card,
b input from m/s 18 in the "one-to-the-east" tiling card, and
a input from m/s 23.



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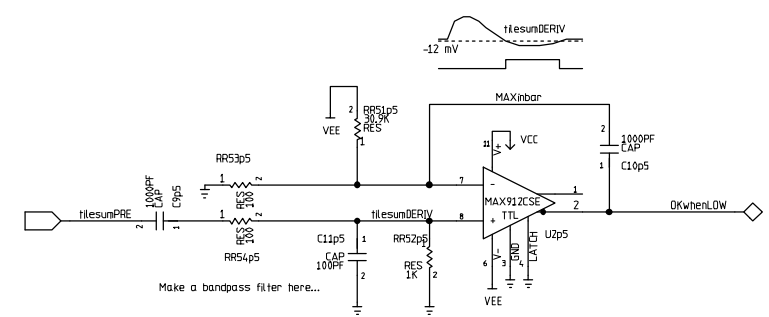
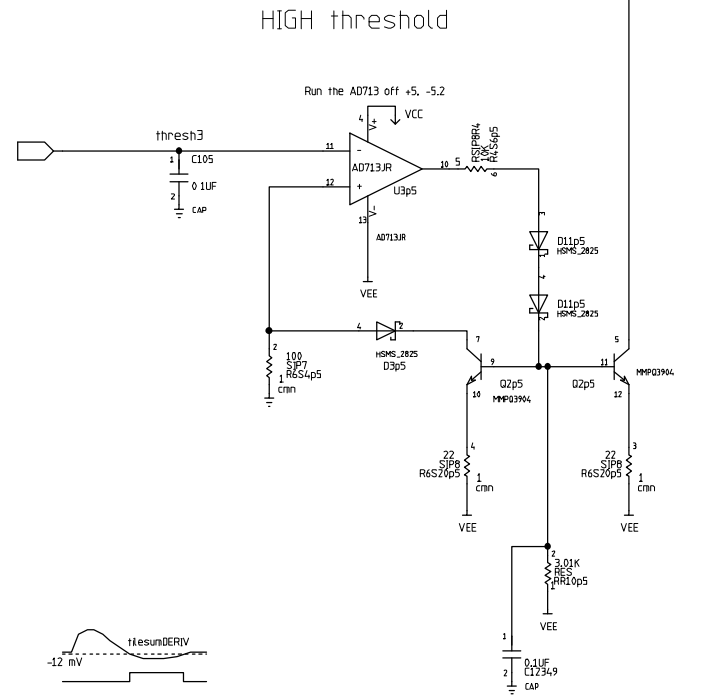
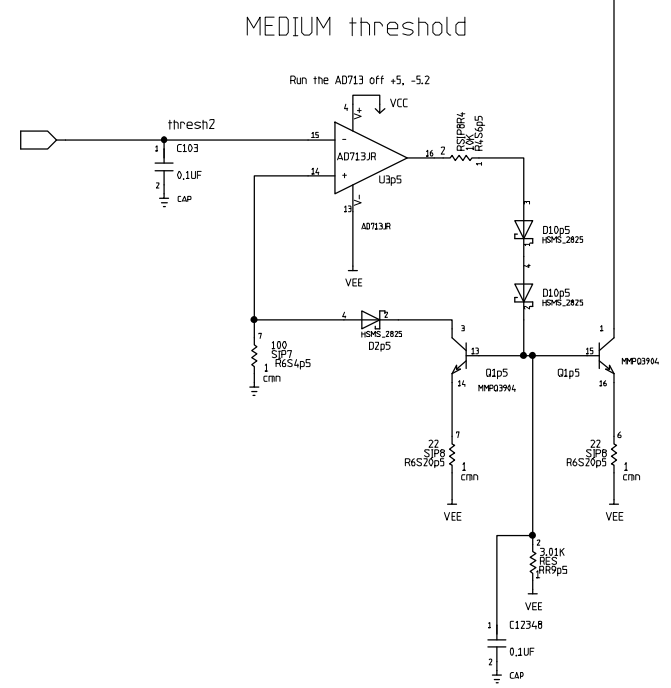
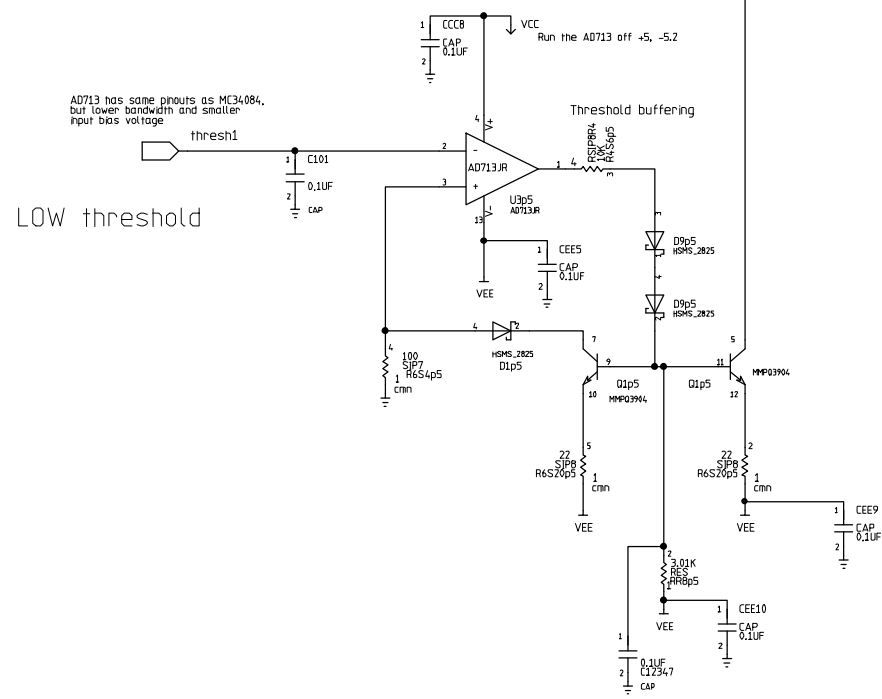
Note: AD9698 and MAX912CSE are dual comparators, so the V+ V- pins are duplicated on each symbol. As a result, place the bypass capacitors separately V+ = +5, V- = -5.2.



HP HMS-2825 is a Schottky diode, packaged two per SOT-143 package. Use diodes in the same package for matching.

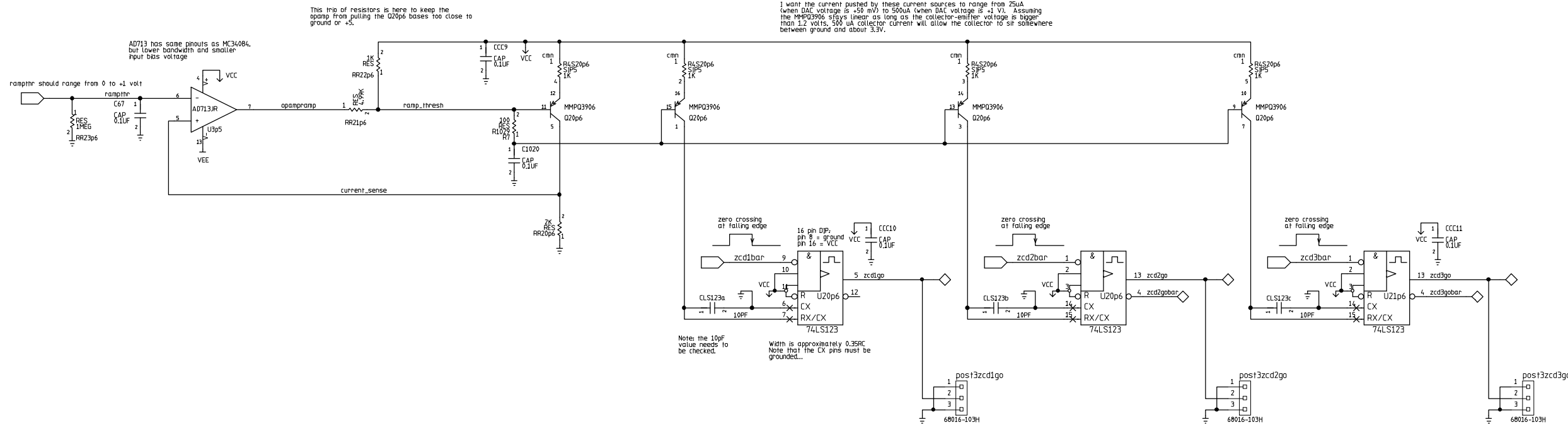
5% COG ceramic cap

5% COG ceramic cap

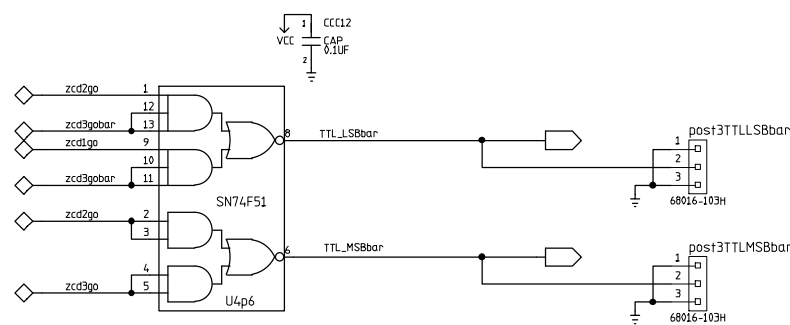


Use this MAX912 to check that we aren't in the middle of a large pulse, and on the back side (where the slope is negative). If we are, block the low and medium threshold pulses.

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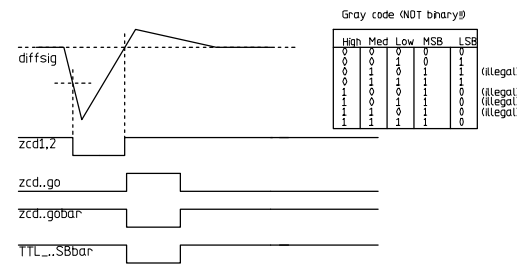


NOTE: remove the nested CCT name "SN74LS123" property from the 74LS123's before doing PCB layout.



Generate Gray codes here (NOT binary!!!)

TTL_MSBbar is NOT (zcd2go OR zcd3go)
TTL_LSBbar is NOT (zcd1go AND zcd3gobar) OR (zcd2go AND zcd3gobar)



TTL_MSBbar is NOT (zcd2go OR zcd3go)
TTL_LSBbar is NOT ((zcd1go AND zcd3gobar) OR (zcd2go AND zcd3gobar))

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