

# The CLEO-III Trigger: Analog and Digital Calorimetry

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# Outline

## CLEO-III trigger description

- What's new since CLEO-II.5
- Signal path: calorimeter → trigger
- Analog processing
- Digital processing

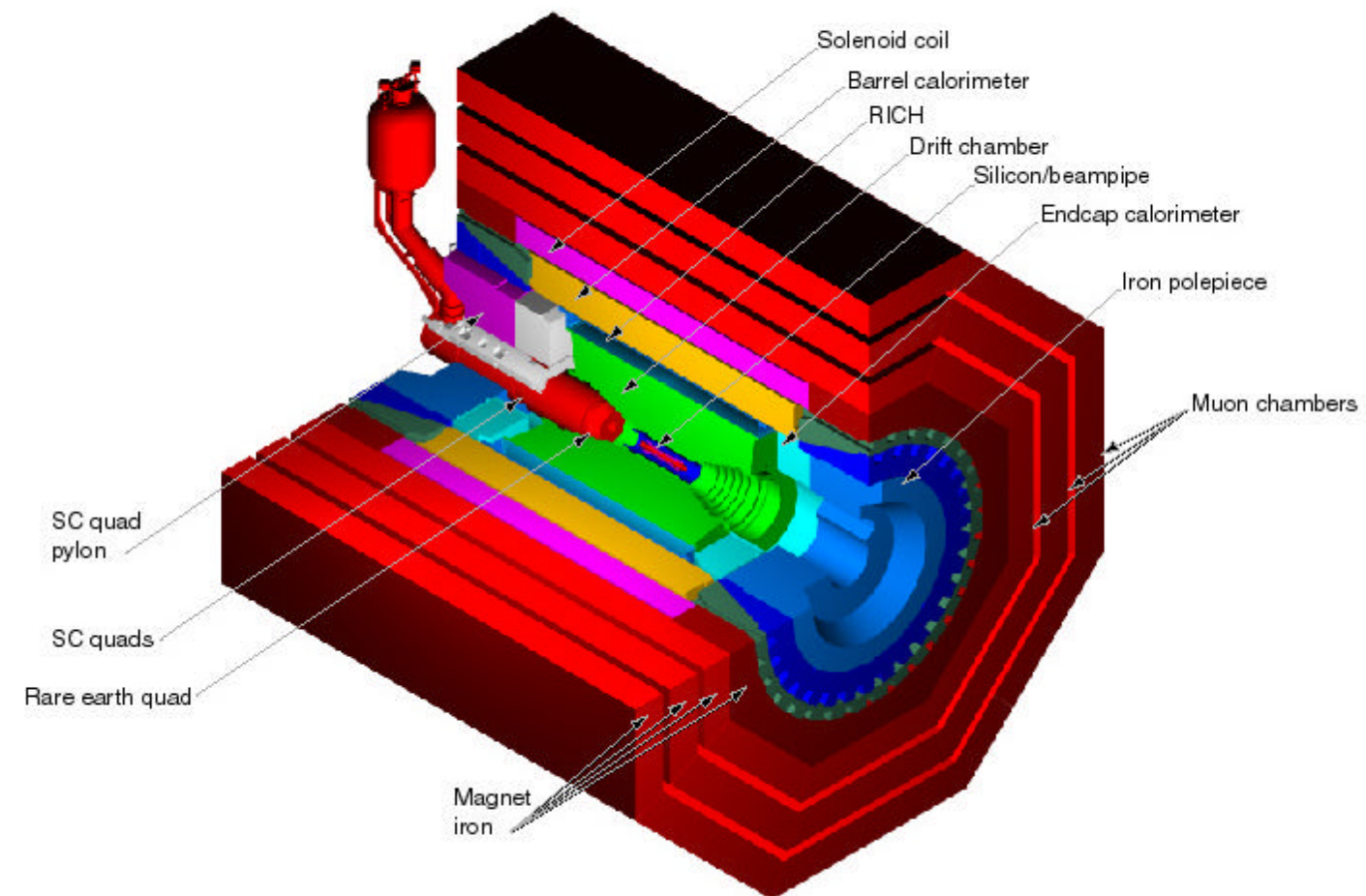
## Neat analog stuff

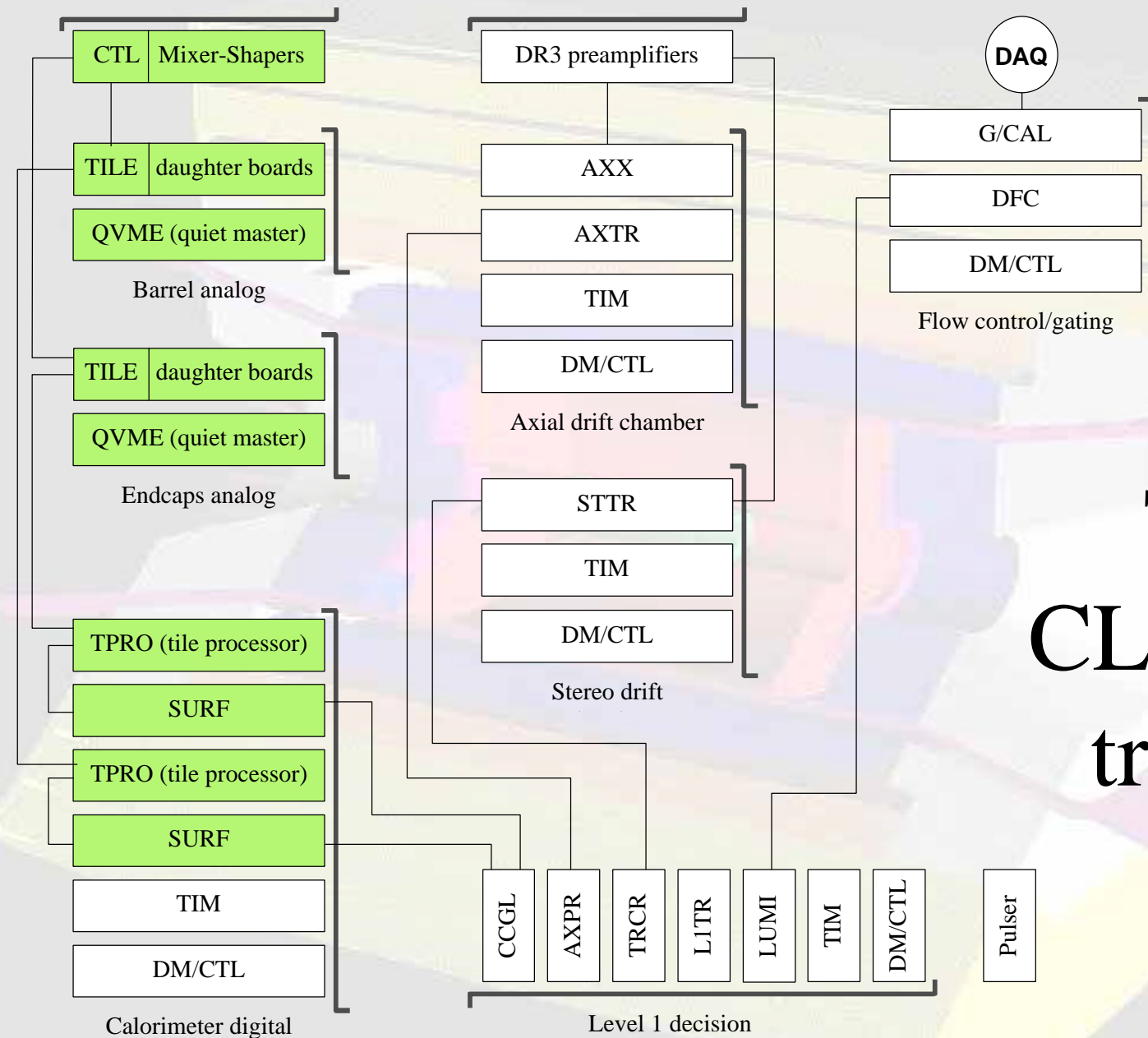
- self-test capability
- gain adjustments
- output pulse width control

## Wrinkles

See: <http://web.hep.uiuc.edu/cleo/trig3/boards/>  
<http://web.hep.uiuc.edu/cleo/trig3/boards/TILE/>

# CLEO-III detector



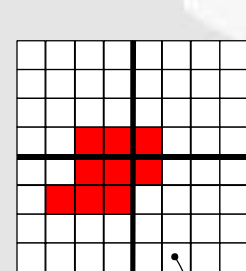


# The CLEO-III trigger

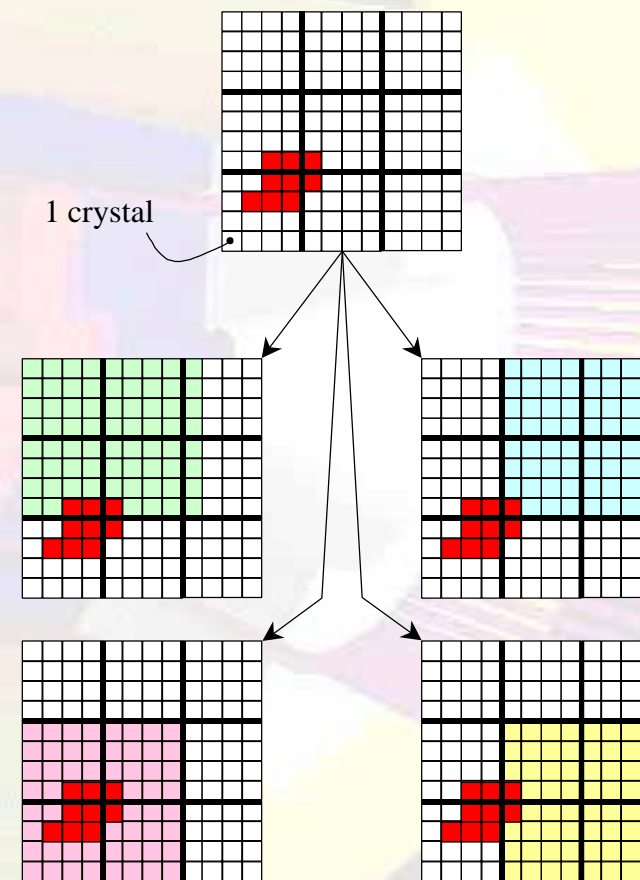
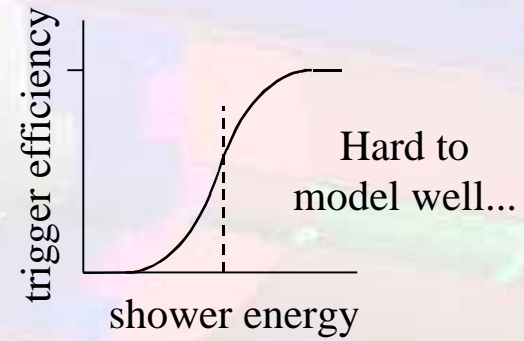
# CLEO-II vs. CLEO-III

CLEO-II

CLEO-III

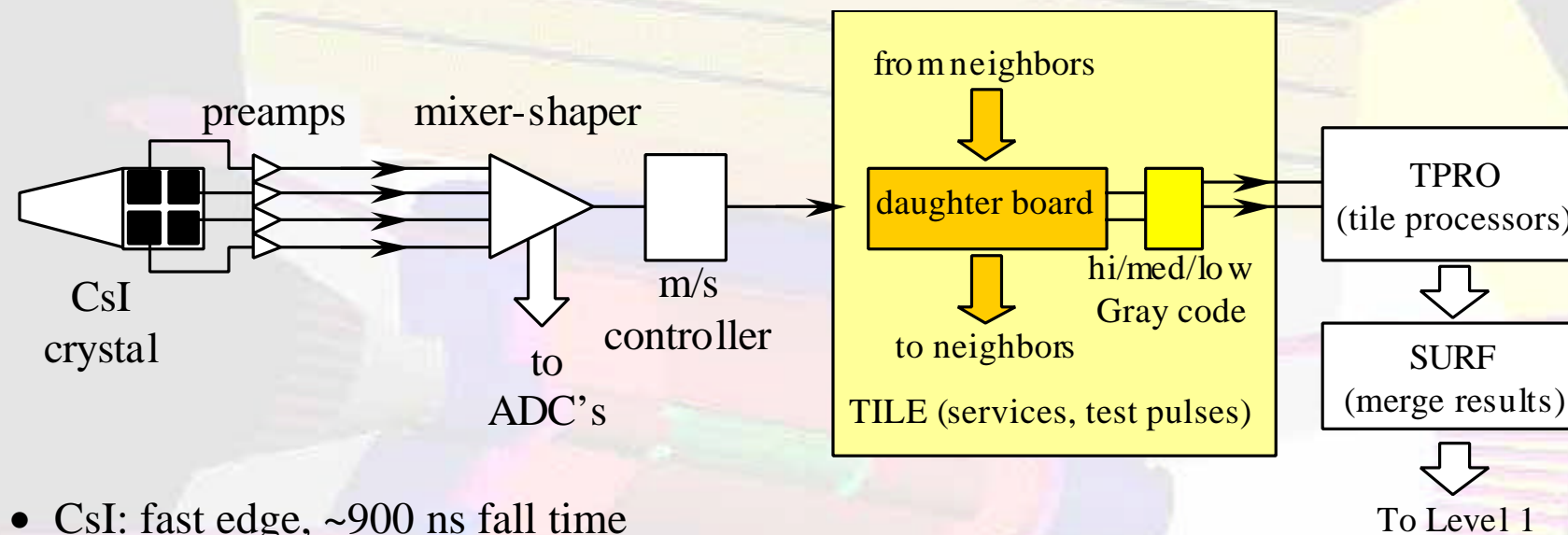


1 crystal

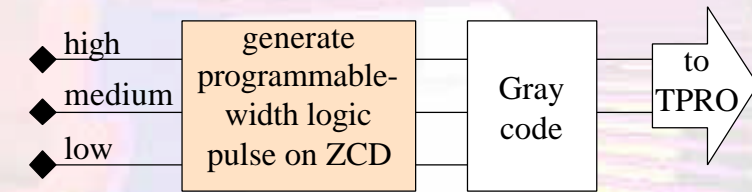
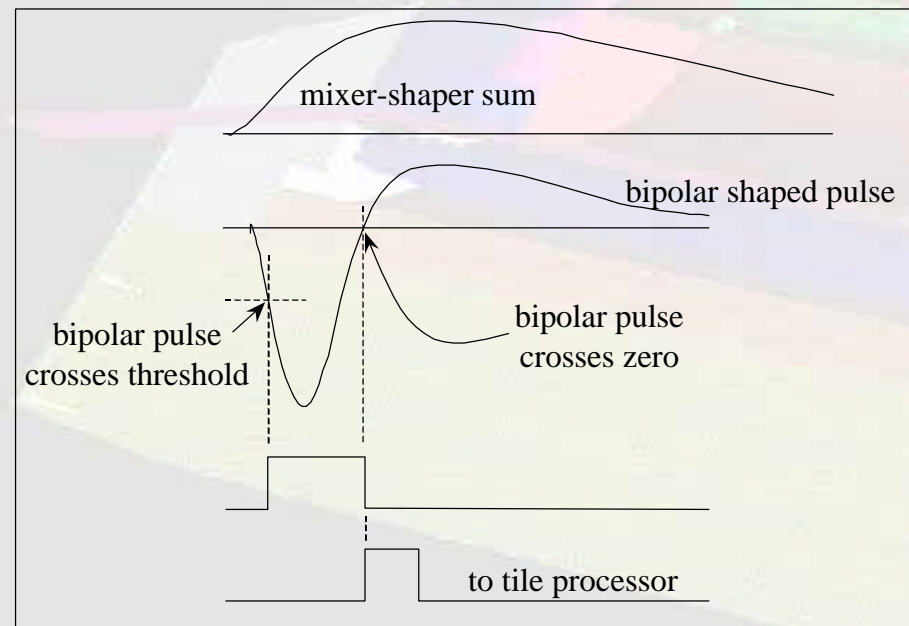
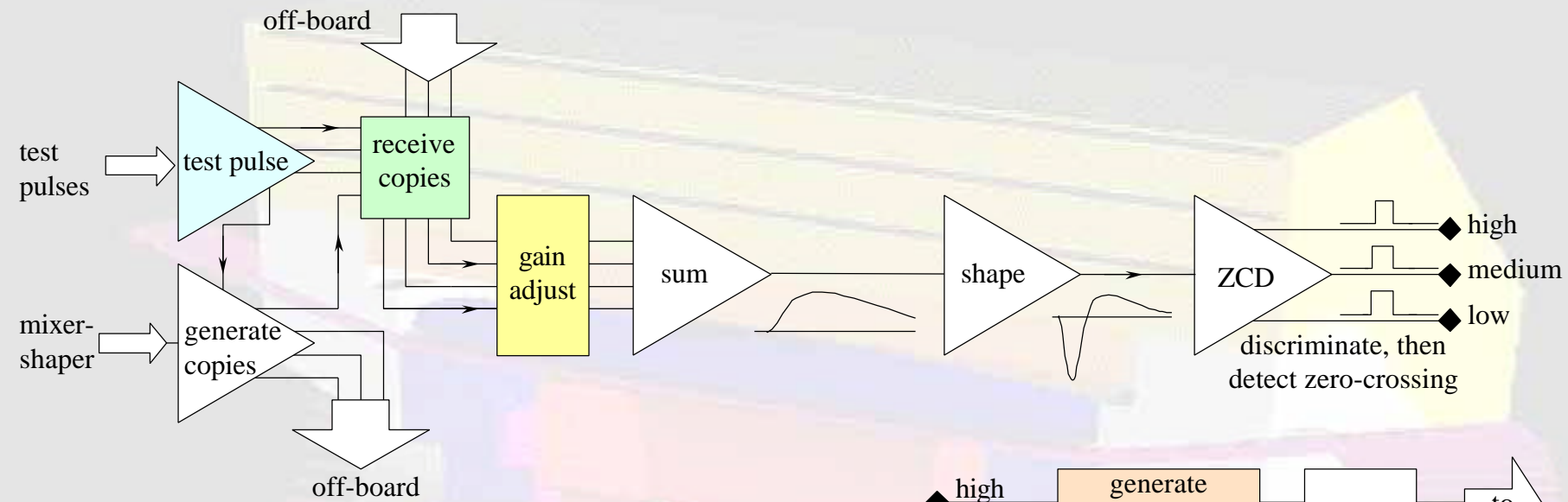


Showers spanning boundaries between regions in the CLEO-II calorimeter were difficult to simulate precisely. For CLEO-III, which forms analog sums of overlapping regions, at least one “tile” will contain the entire shower.

# Signal path for one CsI crystal

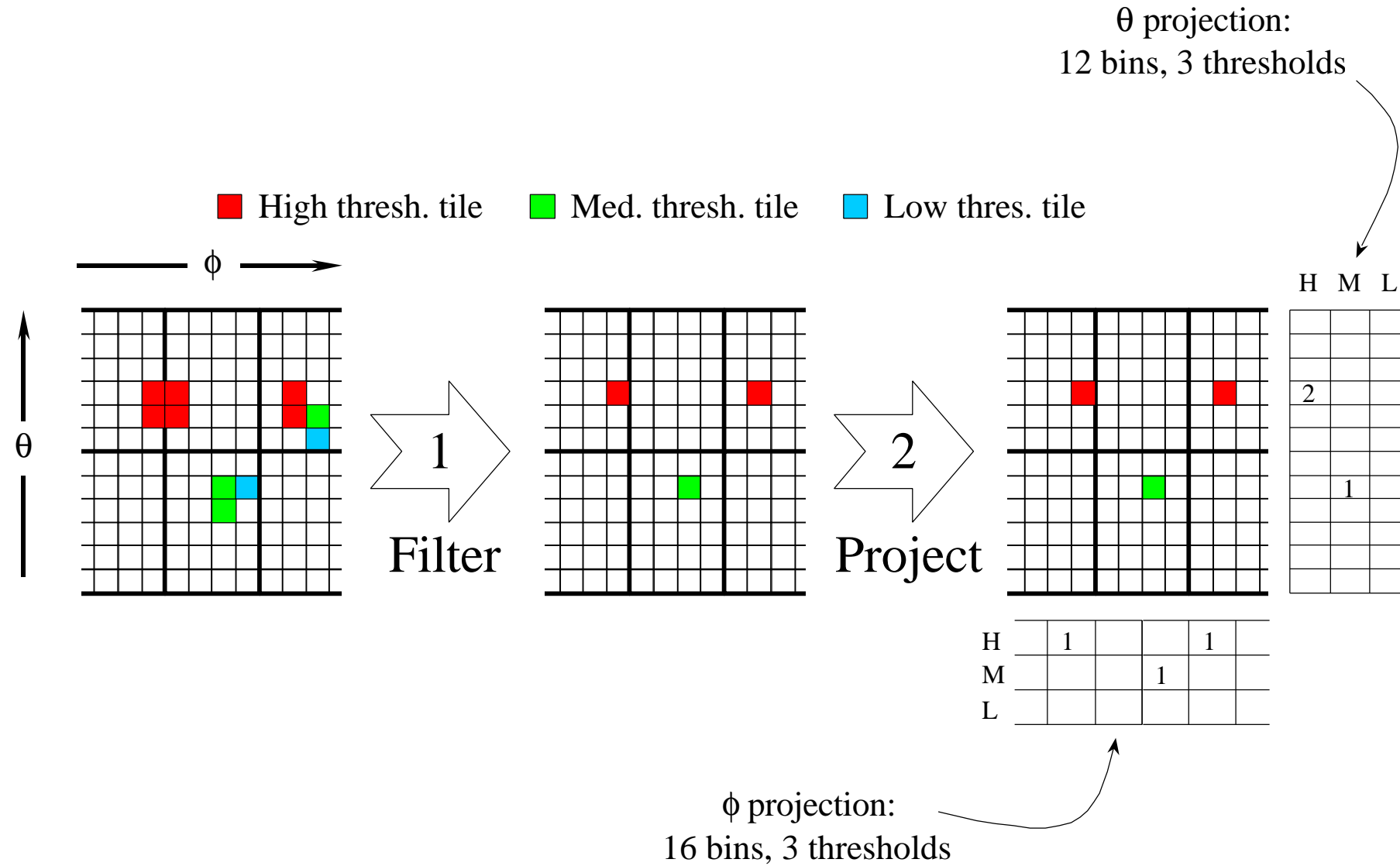


- CsI: fast edge,  $\sim 900$  ns fall time
- Preamp: peak  $\sim 3$   $\mu$ s, fall  $\sim 180$   $\mu$ s.
- M/s controller: peak  $\sim 2.5$   $\mu$ s, fall  $\sim 8$   $\mu$ s.
- Daughter board copies its mixer-shaper signal to neighbors
- Daughter board sums 4 analog signals
- Summed signal shaped (bipolar), then discriminated.
- Signals  $>$  hi/med/lo thresholds: zero-crossing-synched logic pulses sent to tile processors.
- Results from tile processors (4 barrel, 2 endcap) combined by SURF boards, then sent to Level 1 trigger.

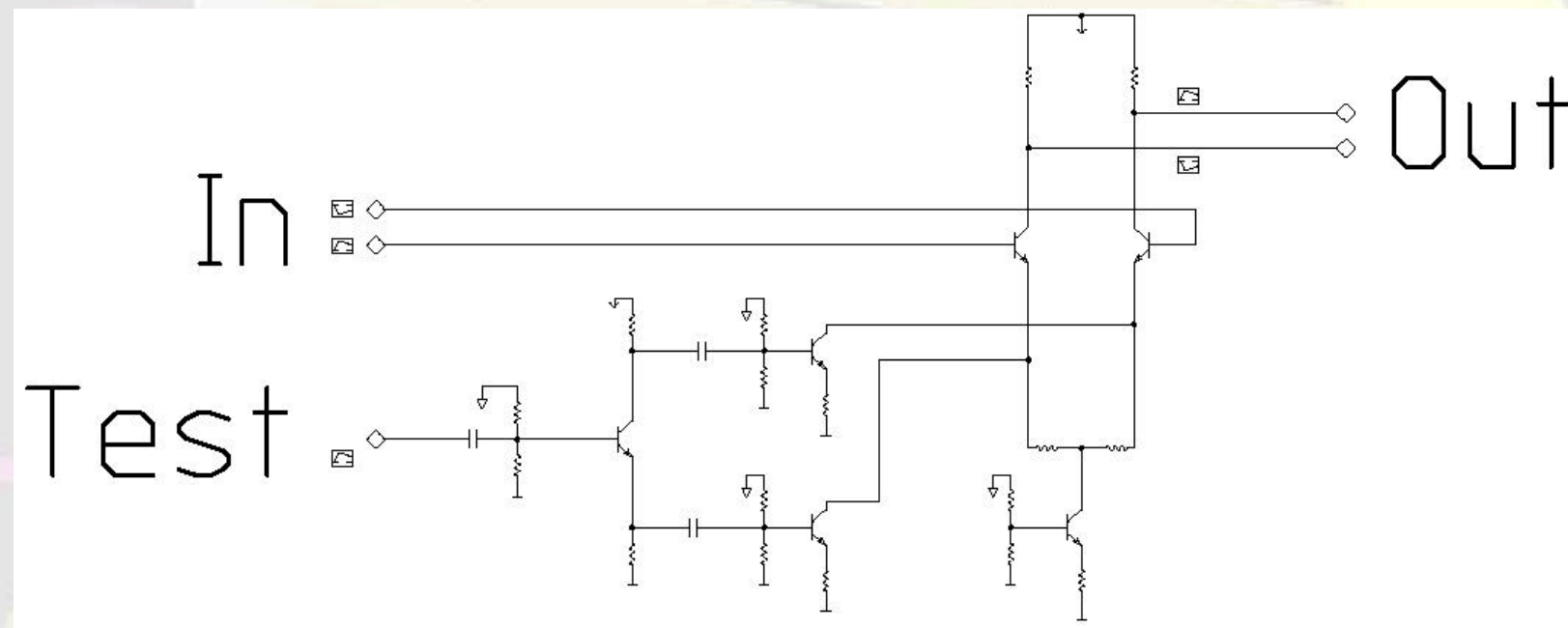


# CLEO-III daughter board

# Tile processing steps

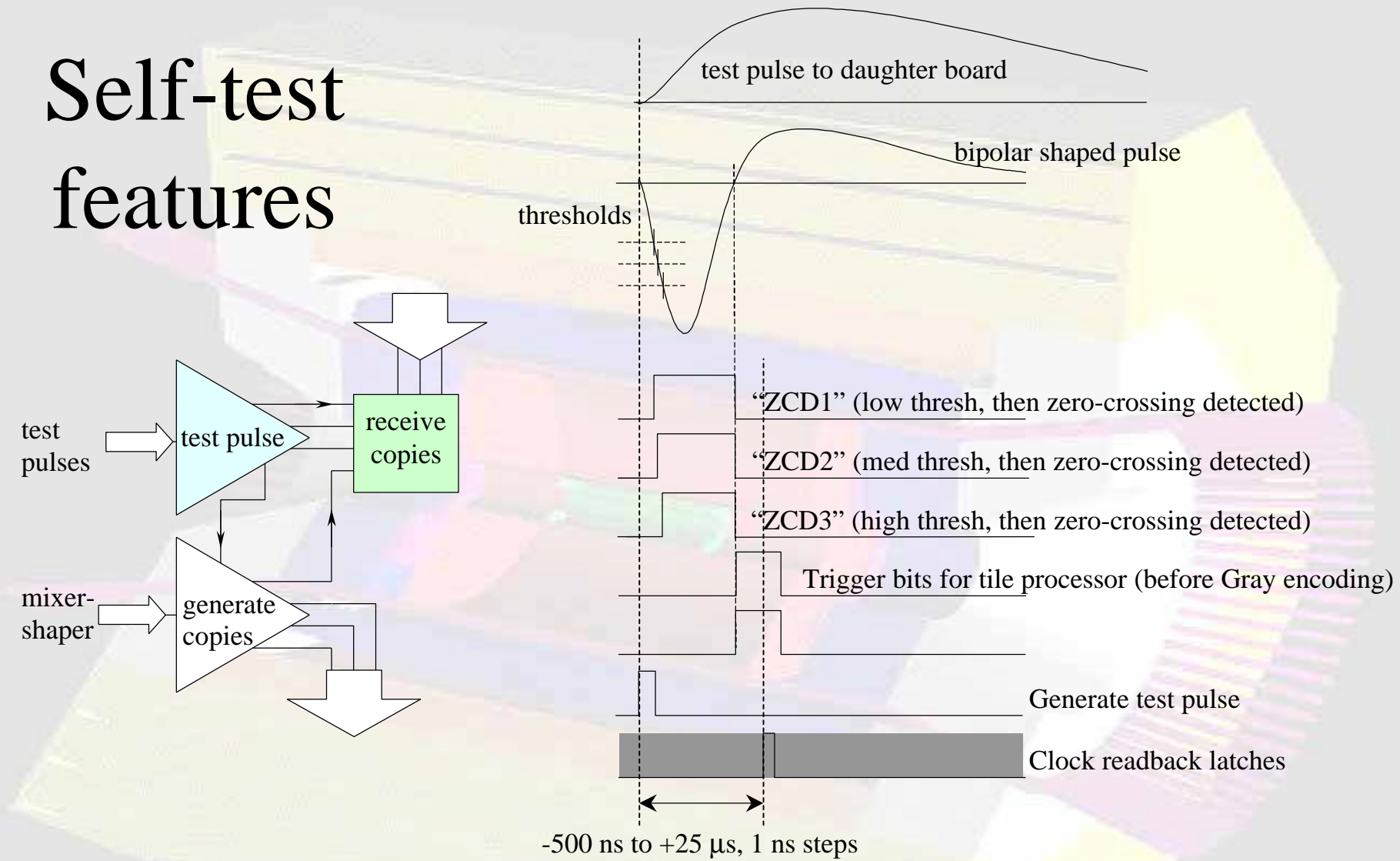


## Self-test features



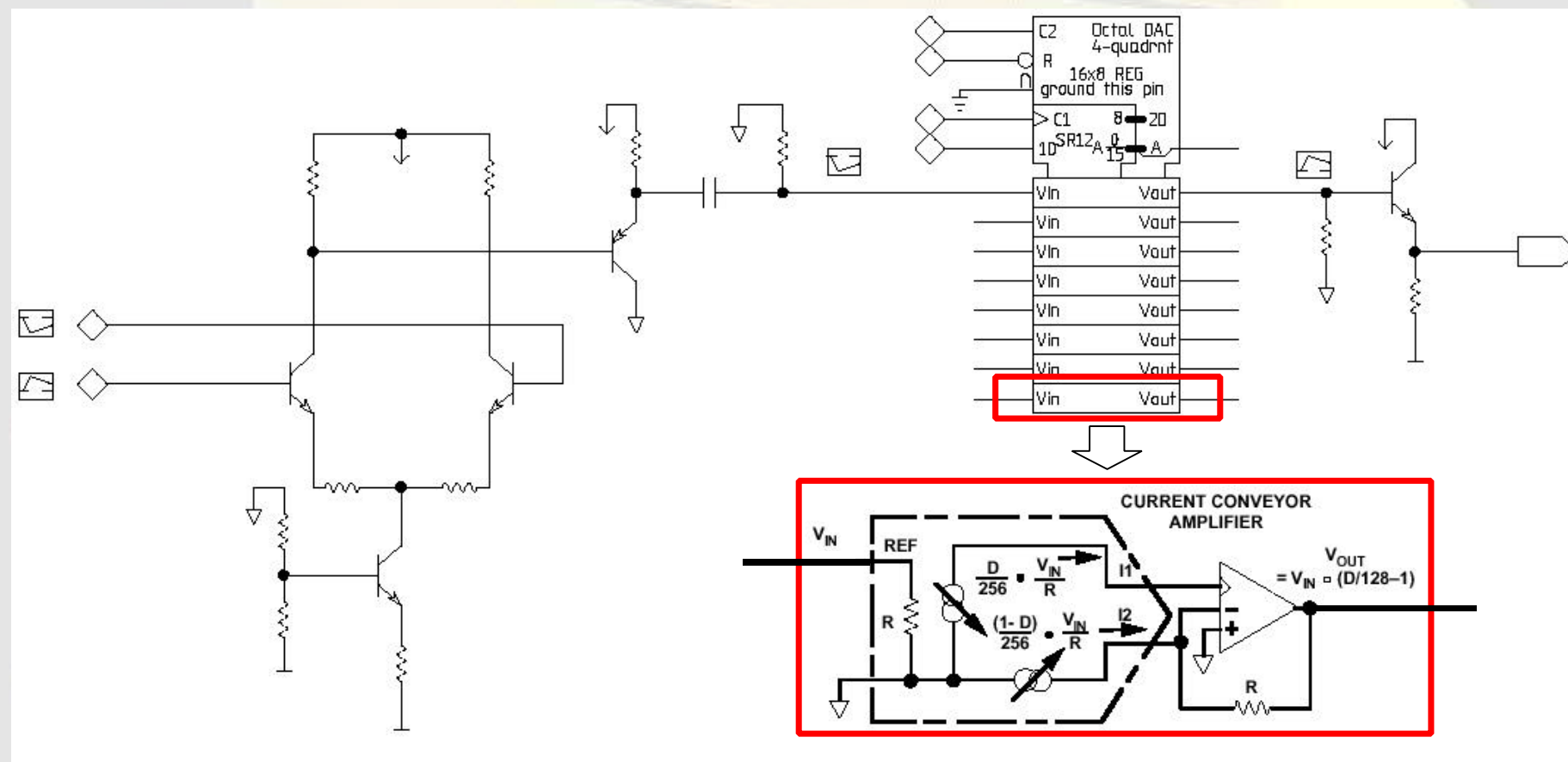
Inject realistic test pulses into input transistors so that full signal path is driven...

# Self-test features



Vary test pulse - latch clock delay and thresholds to test boards:  
discriminator + threshold DAC = ADC

# Gain adjustments...



Analog Devices AD8842 TrimDAC

# Gain adjustments...

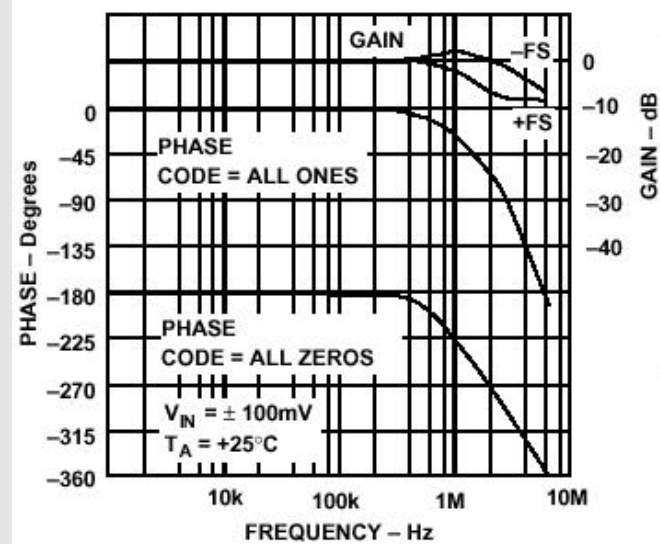


Figure 10. Gain and Phase vs. Frequency (Code = 00<sub>H</sub> or FF<sub>H</sub>)

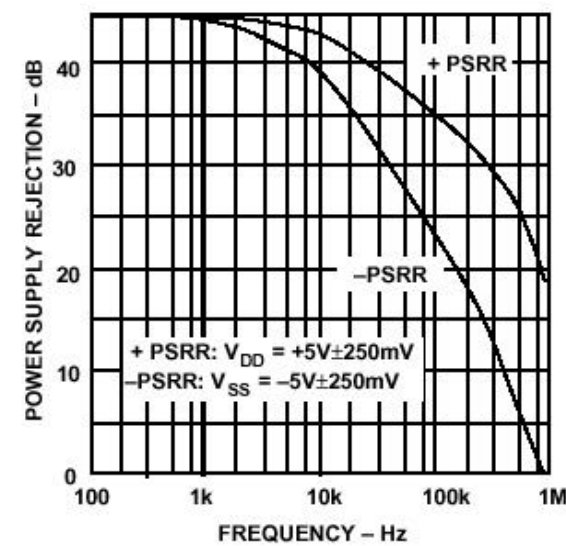


Figure 23. PSRR vs. Frequency

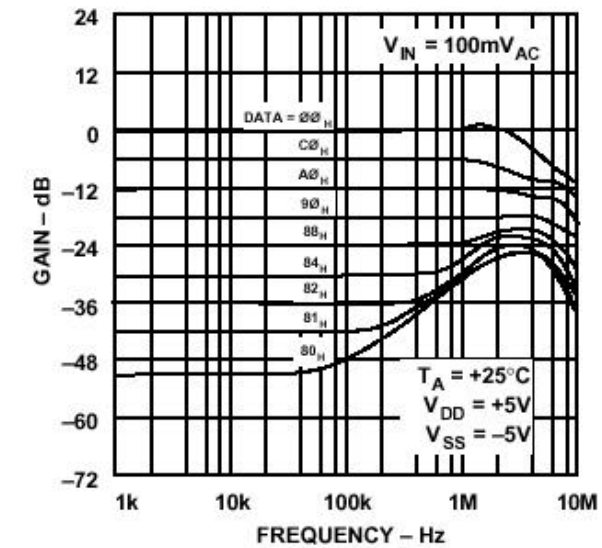
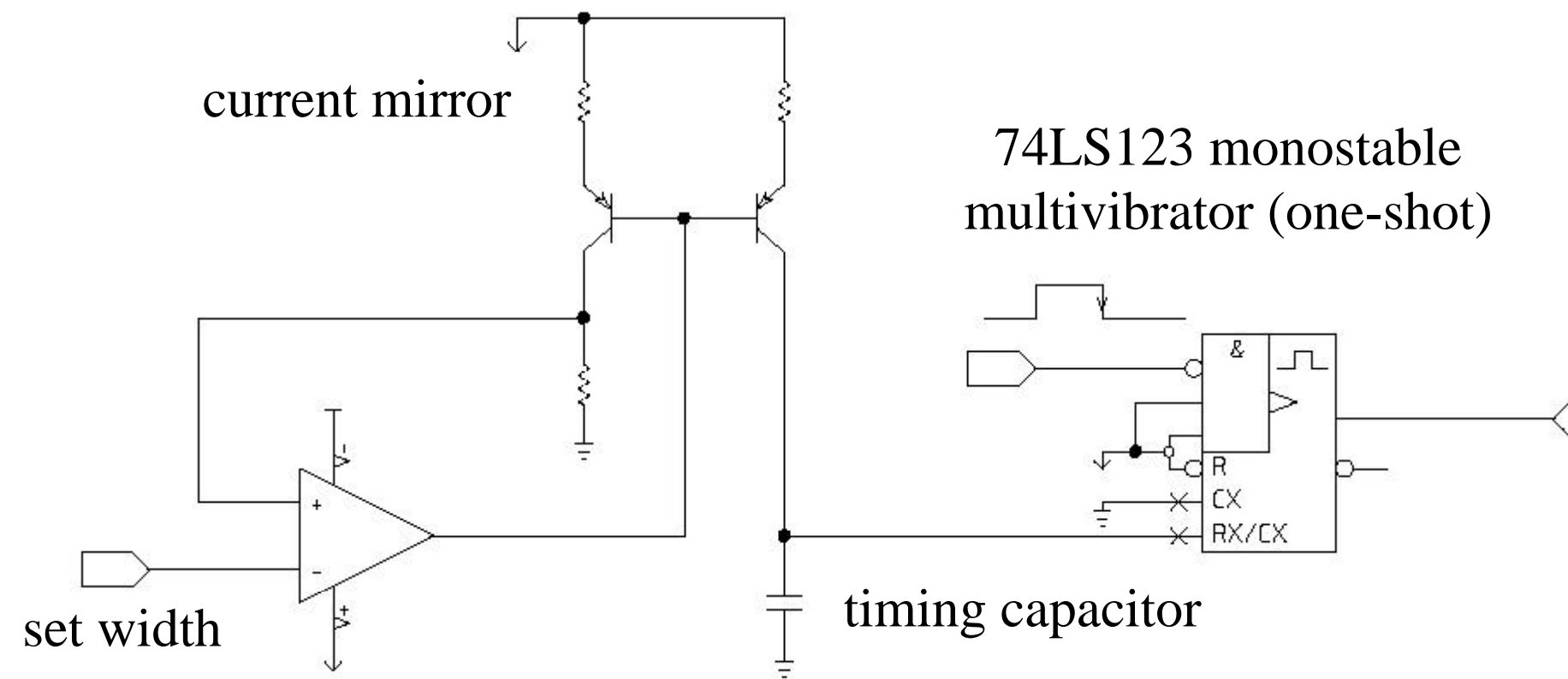


Figure 24. Gain ( $V_{OUT}/V_{IN}$ ) and Feedthrough vs. Frequency

AD8842: very nice device, ~1 € per channel, but be careful...

# Output pulse width programming



# Life is always interesting...

Noise environment hard to predict before installation.

- ~4 MHz common-mode glitch at 60 Hz
- coherent noise upstream of sum
- high frequency supply noise in full system  
(PSRR drops at high frequencies)

Lots of ferrite toroids on cables to block common mode noise...

Grounds are hard for physicists to understand: confusion over IR vs.  $I\omega L$  voltage differences, etc. etc.

# Life is always interesting...

Parts didn't always behave like we expected:

- touchy (non-Maxim) discriminators
- correct configuration data shift / load / clear algorithm is different from documentation
- surprising (mixed signal) device sensitivity to noise on digital inputs

Mixed signal (analog/digital) boards are tricky: board layout is important.

Experimental halls flood, submerging spare boards temporarily kept in boxes on the floor

## Art simulates life...

Good analog simulation tools, well-integrated with circuit design capture, proved invaluable.

User interface could be improved.

Often, SPICE models for new devices don't exist.

Including layout information in simulation can be complicated.

## We're working on it...

System has not been in use for very long. We are currently investigating:

- relative timing for signals passed from neighboring daughter boards *vs.* directly from mixer-shapers
- noise associated with analog signals passed across VME crate boundaries

Built for CLEO-III calorimeter trigger:

- ~700 daughter boards
- ~30 TILE boards
- ~30 mixer-shaper controllers
- ~8 tile processor boards
- ~8 QVME
- ~4 SURF...