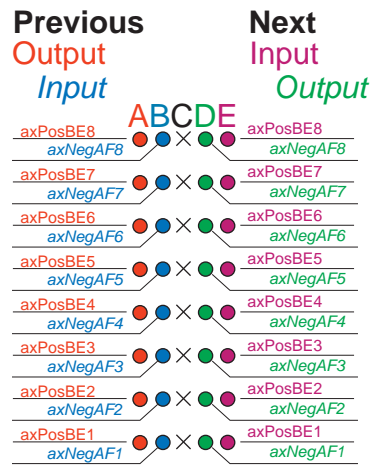


Backplane connector for the STTR.
000216-CLP
logical layout
BACKPLANE
(as seen from inside
STTR crate).

Chips used
Bigor3
outputchip

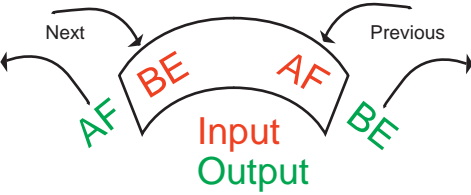
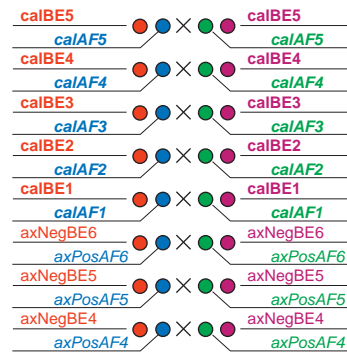
P5
1 (4)
2 (5)
3 (6)
4 (7)
5 (8)
6 (9)
7 (10)
8 (11)



BigOr and Outputchip:

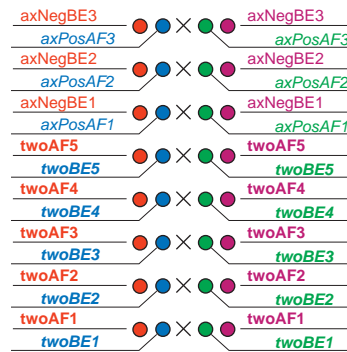
Bigor1
Bigor3
outputchip
Bigor1
Bigor2
outputchip

12 (15)
13 (16)
14 (17)
15 (18)
16 (19)
17 (20)
18 (21)
19 (22)



Bigor1
Bigor2
outputchip
shareA

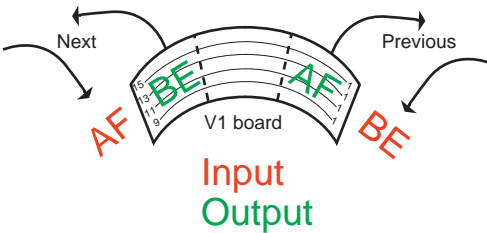
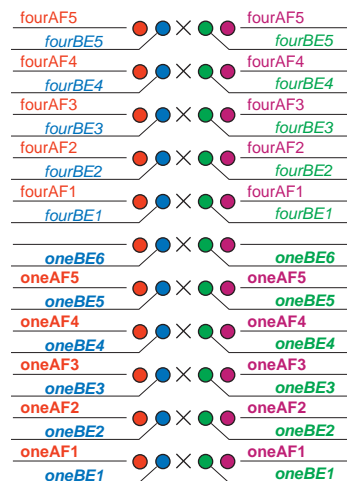
P6
26 (4)
27 (5)
28 (6)
29 (7)
30 (8)
31 (9)
32 (10)
33 (11)



Sharing:

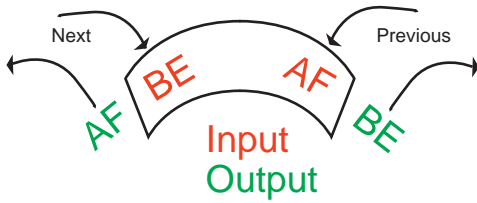
shareA
shareB

37 (15)
38 (16)
39 (17)
40 (18)
41 (19)
42 (20)
43 (21)
44 (22)
45 (23)
46 (24)
47 (25)



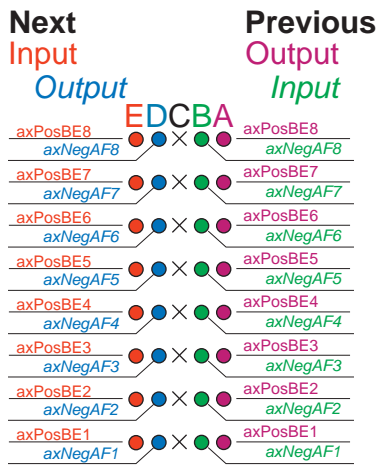
Backplane connector for the STTR.
 000216-CLP
 logical layout
 FREE BOARD
 (this is also the layout of the backplane from behind the STTR crate).

BigOr and Outputchip:



Chips used
 Bigor3
 outputchip

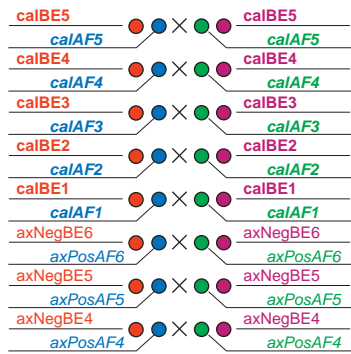
- P5
- 1 (4)
- 2 (5)
- 3 (6)
- 4 (7)
- 5 (8)
- 6 (9)
- 7 (10)
- 8 (11)



Bigor1
 Bigor3
 outputchip

Bigor1
 Bigor2
 outputchip

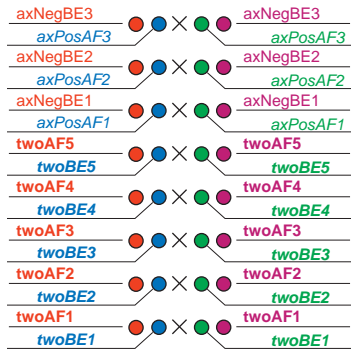
- 12 (15)
- 13 (16)
- 14 (17)
- 15 (18)
- 16 (19)
- 17 (20)
- 18 (21)
- 19 (22)



Bigor1
 Bigor2
 outputchip

shareA

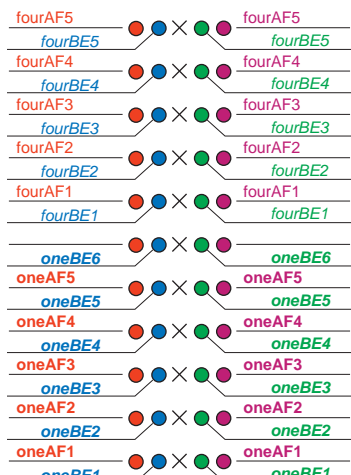
- P6
- 26 (4)
- 27 (5)
- 28 (6)
- 29 (7)
- 30 (8)
- 31 (9)
- 32 (10)
- 33 (11)



shareA
 shareB

shareB

- 37 (15)
- 38 (16)
- 39 (17)
- 40 (18)
- 41 (19)
- 42 (20)
- 43 (21)
- 44 (22)
- 45 (23)
- 46 (24)
- 47 (25)



Sharing:

