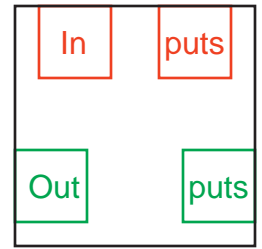


# Backplane Summary

STTR p5/p6 backplane 000216 - CLP



## PRE-Logic (one, two, four; Sharing)

INPUTS (Sharing):

Previous board -> BEfore

Next board -> AFter

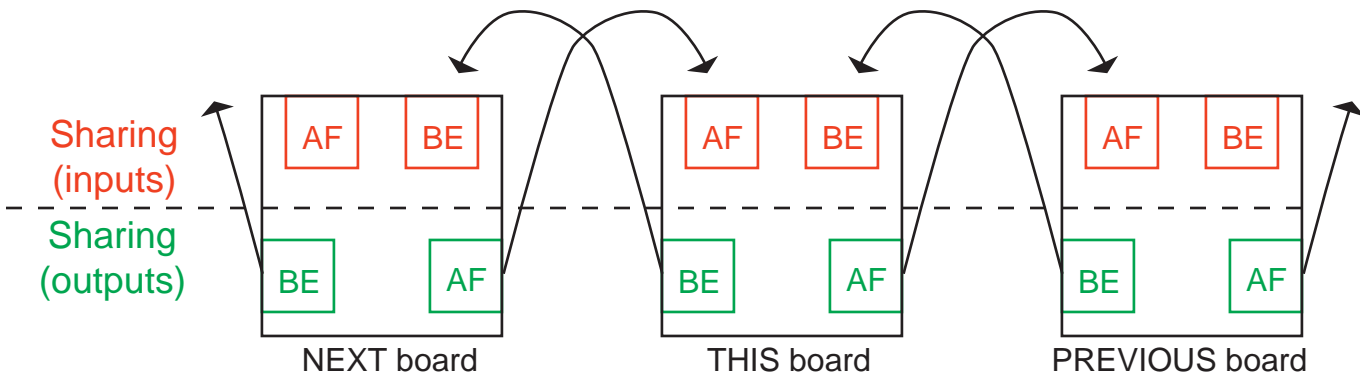
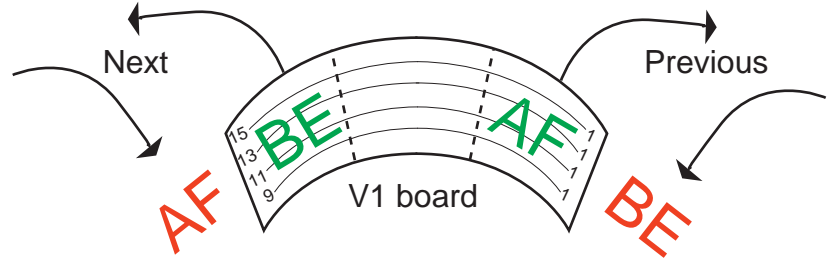
OUTPUTS (Sharing):

BEfore[5..1] = four[11..15]

AFter[5..1] = four[5..1]

BEfore -> Next board

AFter -> Previous board



## POST-Logic (axPos, axNeg, cal; BigOr and OutputChip)

INPUTS (OutputChip):

Previous board -> AFter

Next board -> BEfore

OUTPUTS (BigOr):

BEfore -> Previous board

AFter -> Next board

