

## 2. Mother board modifications

Modifications to the mother board circuit are intended to reduce the self-test circuit's noise sensitivity and to reduce the maximum delay between generation of a test pulse and firing of the read-back latches used to register the states of the five TTL lines brought off each daughter board. The modifications involve the following:

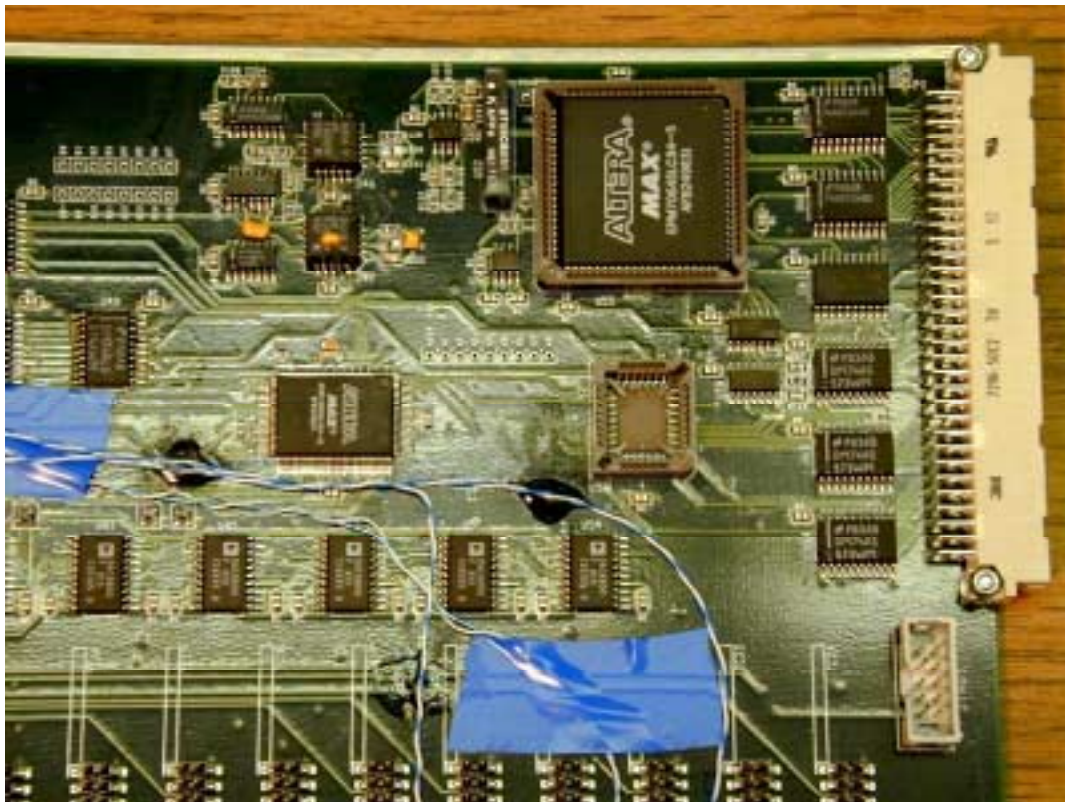
1. soldering a 100 pF leaded capacitor between pins 2 (latch clock) and 20 (ground) of chip U47 (an AD9501 delay generator) to reduce its sensitivity to noise on its digital input line
2. removal of chip capacitor C232, located just to the right of U47
3. installation of a 220 pF leaded capacitor between the left-side pad where C232 had been and the ground side (right side) of R120, also located just to the right of U47.
4. replacement of chip capacitor C204 (above U42, very close to the top edge of the board) with a 220 pF chip capacitor.

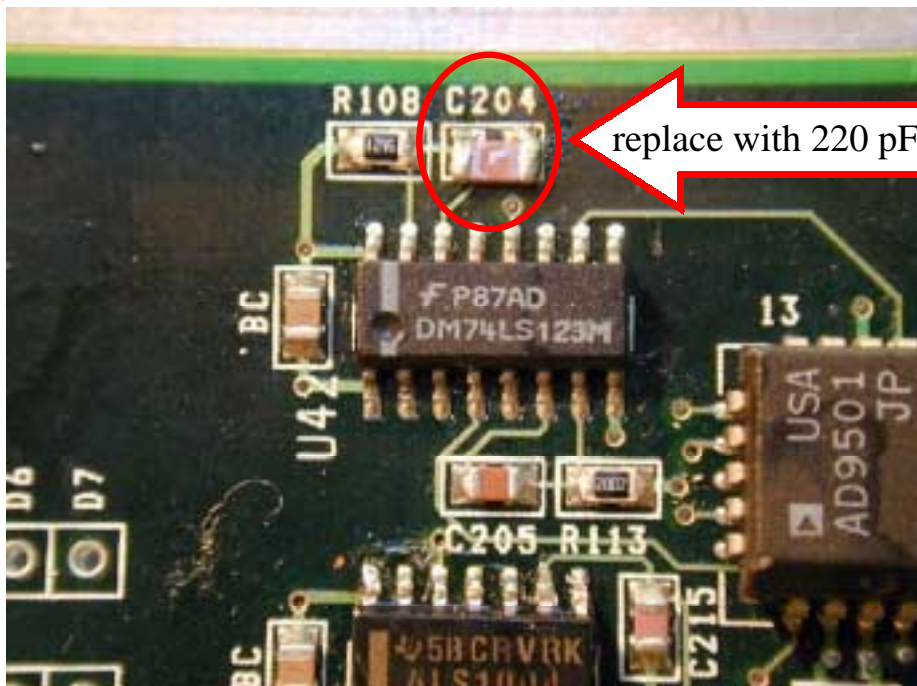
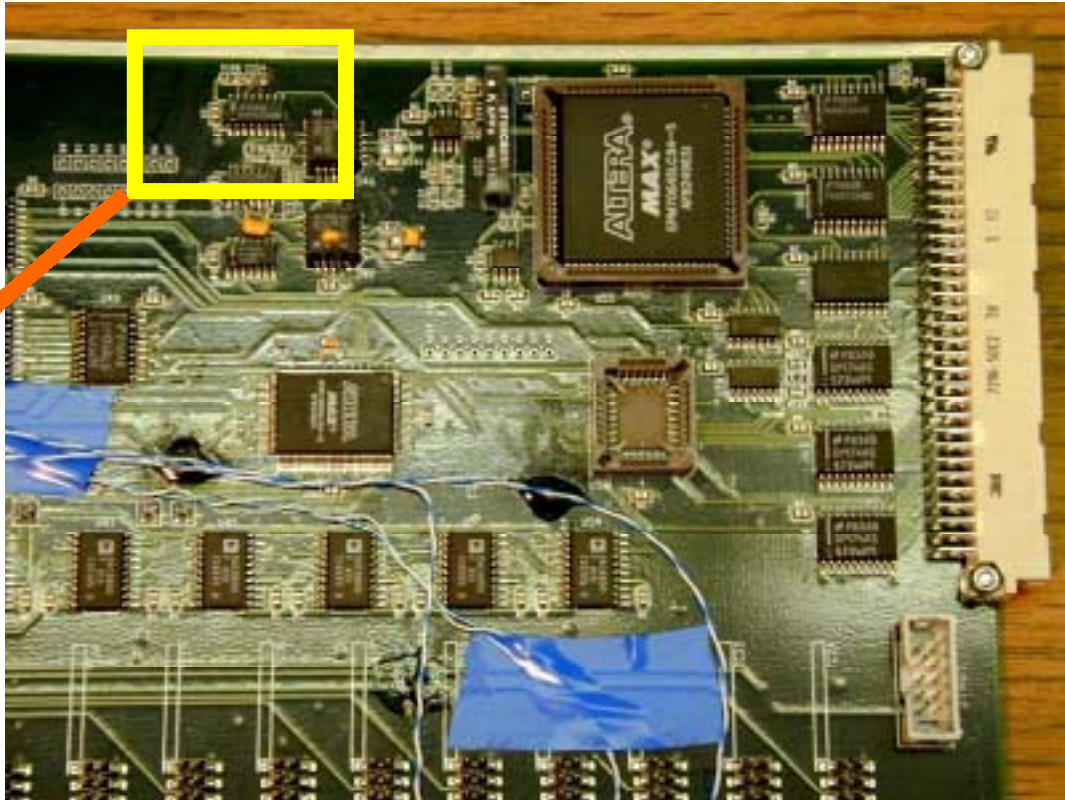
Modification 1 reduces the AD9501's sensitivity to noise on its digital input line which can introduce jitter into the delay it generates.

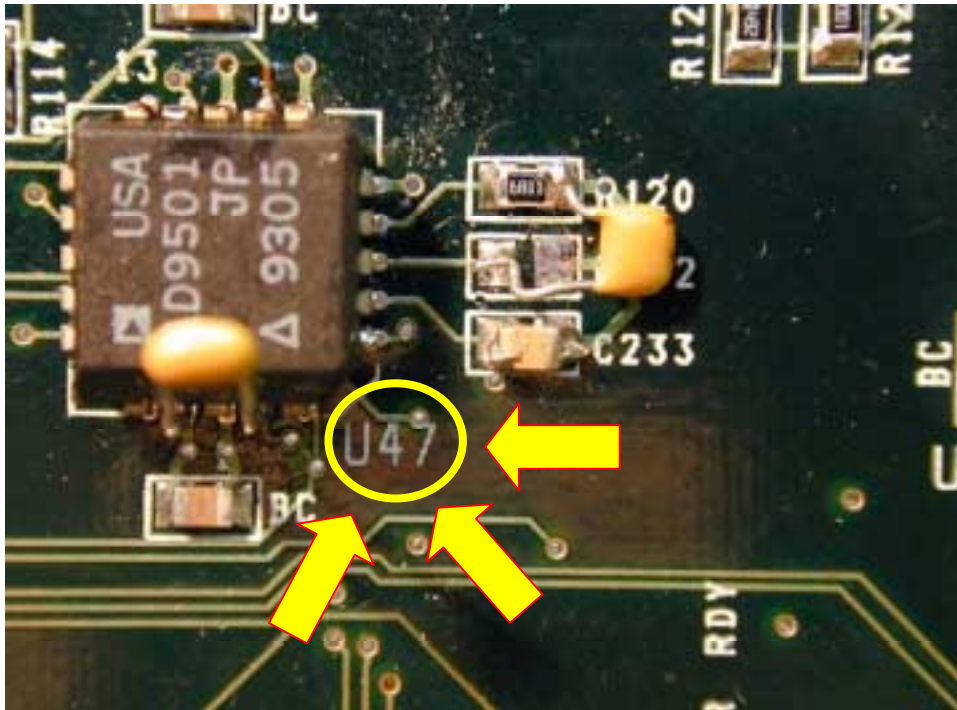
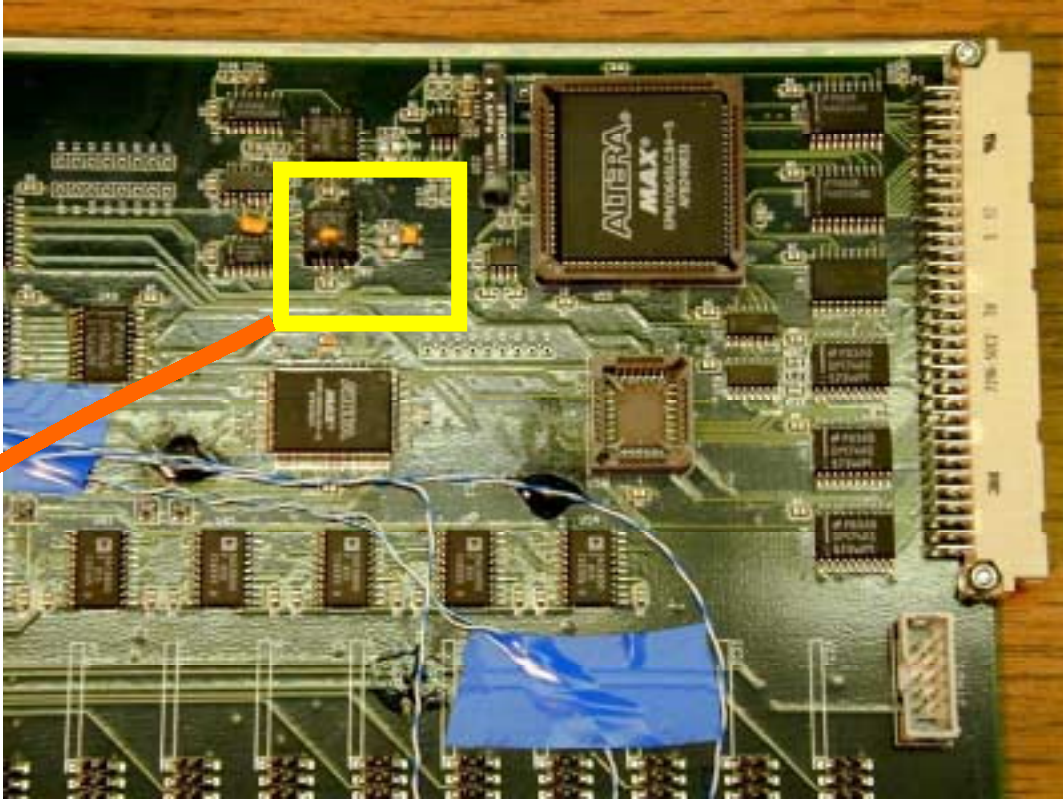
Modifications 2 and 3 reduce the maximum delay generated by the AD9501.

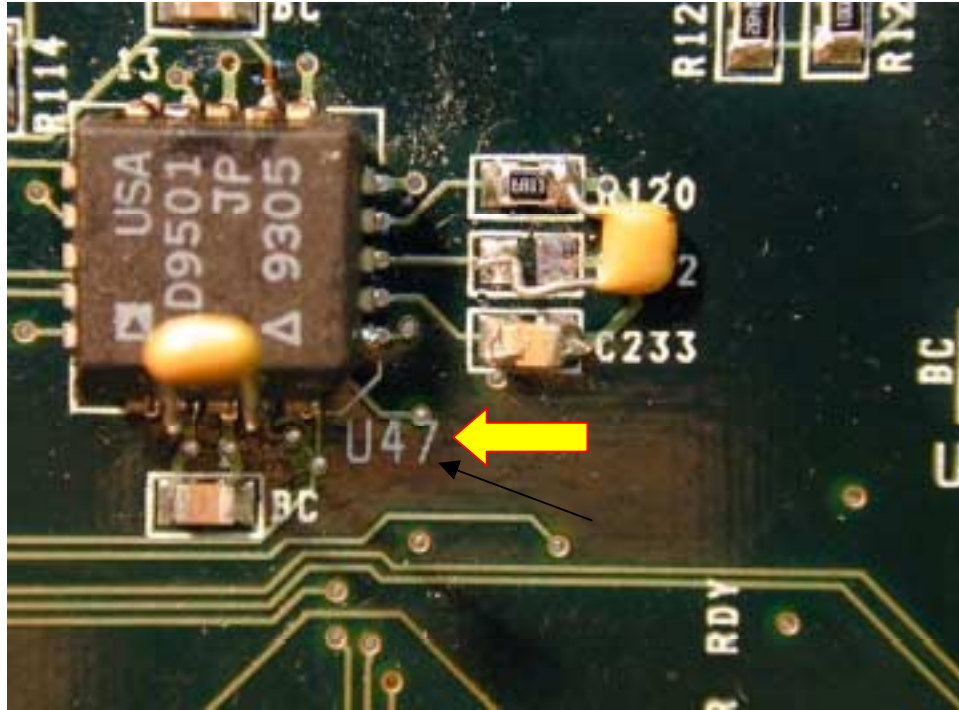
Modification 4 adjusts the minimum delay between firing of the latch gate and the generation of a test pulse by reducing the width of the output from a timing one-shot (74ls123).

New Parts: one 100 pF leaded capacitor, one 220 pF leaded capacitor, one 220 pF 805 capacitor per mother board.









Be sure you are modifying the U47 AD9501.

