

## Vertex Detector Table of Contents

Table of Contents and Overview .....	4.0
A Proposal for R&D on CCD Vertex Detectors for Future Linear e+ e- Colliders .....	4.1
Development and design of an LC ASIC for CCD readout and data reduction .....	4.2
Study of the Mechanical Behavior of Thin silicon and the Development of hybrid silicon pixels for the LC .....	4.3
Investigation of new technologies for the silicon vertex tracker .....	4.4

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### Vertex Detector Proposals Overview

The precision determination of Higgs couplings, efficient flavor tagging in multi-jet events, and determination of heavy quark charge all benefit by pushing vertex detector performance to new levels. The linear collider environment, with its centimeter radius beam pipe, low event rates, and low radiation fields, admits vertex detectors that are substantially thinner, more precise and more segmented, and significantly closer to the IP than vertex detectors at the LHC. But R&D is required. CCD vertex detectors have already demonstrated very high resolution and segmentation, moderate multiple scattering, rather low radiation hardness, and slow readout. To apply CCD technology to the LC will require much improved radiation hardness and a factor 100-1000 increase in readout speed. Thinning the detectors may also be important. Other technologies, including hybrid pixel detectors, are sufficiently radiation hard and can be read out rapidly, but are much thicker (hence worse multiple scattering) and have coarser segmentation, hence poorer resolution and immunity to backgrounds. The physics benefit of pushing to very thin designs has not been fully quantified as yet, and may be important in selecting the optimal technology.

The vertex proposals submitted below address the outstanding R&D issues. The Oregon/Yale (A) and Boston University/Oklahoma/FNAL (B) proposals focus on CCD technology. They address characterizing and improving radiation hardness, developing new and faster CCDs, and improving CCD readout schemes, as well as thinning and supporting thinned CCDs. The Purdue/FNAL (C) proposal includes simulation studies to check the resolution and multiple scattering requirements, and the development of thinner, higher resolution hybrid pixel detectors. All these efforts will be coordinated with other work on the international scene. The Northwestern/FNAL proposal (D) will concentrate on developing a readout system suitable for testing a variety of silicon detectors, and using it to investigate radiation hardness and detector thinning. Their efforts will benefit development of microstrip detectors useful for general tracking, in addition to vertex detection.

A.	LCRD	A Proposal for R&D on CCD Vertex Detectors for Future Linear e+e- Colliders	Charlie Baltay, Jim Brau	U. Oregon Yale U.
B.	UCLC	Development and Design of an LC ASIC for CCD Readout and Data Reduction	Patrick Skubic	U. Oklahoma Boston U.
C.	UCLC	Development of Hybrid Silicon Pixels for the Linear Collider	Daniela Bortoletto	Purdue U.
D.	LCRD	Investigation of New Technologies for the Silicon Vertex Tracker	David Buchholz	Northwestern University

## 4.1. A Proposal for R&D on CCD Vertex Detectors for Future Linear e+ e- Colliders (LCRD)

### Vertex Detector

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Oregon  
Yale

FY 2003: \$50,000

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# A Proposal for R&D on CCD Vertex Detectors for Future Linear $e^+ e^-$ Colliders

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University of Oregon

C. Baltay, H. Neal, D. Rabinowitz

Yale University

## 1. Overview of the Proposed Project

Many studies and designs carried out in the U.S., Europe, and Asia, indicate that the most attractive technology for the high precision vertex detectors for future  $e^+ e^-$  colliders are silicon charge coupled devices (CCD's). Alternate technologies being considered are CMOS pixels and hybrid pixels under development for LHC detectors. CCD's have the advantage of smaller pixels for superior spatial resolution and the possibility of thinner detector layers to minimize multiple scattering which is the factor limiting the resolution of the interesting lower momenta. There are, however, significant questions about the feasibility of using CCD's for the next generation of  $e^+ e^-$  colliders. We consider the following to be the key long lead time R&D issues in resolving these questions:

### a) Increasing the Radiation Hardness of CCD's

The expected radiation dose at the SLC was less than 1 krad for the lifetime of the SLD vertex detector and the CCD's were tested to operate at a dose of 10 krad. The detailed background calculations for the next generation  $e^+ e^-$  colliders indicate an upper limit of 100 krad/10 years, a factor of 100 to 1000 higher than at the SLC. The neutron backgrounds are estimated to be around  $10^9$  neutrons/cm<sup>2</sup>/year, larger than at the SLC by a similar factor. We believe that this increase in radiation tolerance can be achieved by various strategies. Reducing the thickness of the surface silicon dioxide layer will reduce the surface damage to ionizing radiation, and reducing the well size in the pixels will reduce the amount of bulk damage due to neutrons. Furthermore, the use of the sacrificial charge technique will reduce the effect of bulk damage on the charge transfer efficiency. To test the success of these strategies will require the design of new CCD's, the fabrication of these devices by commercial silicon fabrication houses, and radiation testing the resulting CCD's.

### b) Decreasing the Readout Time

For the NLC the CCDs have to be read out in the 8.3 msec interval between trains of 190 bunches spaced at 1.4 ns. For TESLA occupancy from a full 2820 bunch train is too large, requiring that partial read out to occur between the 337 ns interval between bunches in the train. For NLC we imagine increasing the

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readout rates to 25-50 MHz (the SLD vertex detector was read out at 5 MHz) and increasing the number of readout nodes to 20 to 40 per CCDs. We believe that this scheme is achievable, but it will require a new CCD design and a prototype CCD fabrication run to test the new design. To achieve the same performance at TESLA, another factor of about 100 would be needed in the product of readout nodes and readout rate.

### c) Reducing the CCD and the Support Structure Thickness

The physics and detector simulation studies carried out over the last several years indicate that the heavy flavor quark tagging ability, which will be so important in the physics of the future  $e^+e^-$  colliders, would be improved if the multiple scattering in the layers of the vertex detector could be reduced to 0.1 to 0.2% of a radiation length. This requires reducing the thickness of the CCD detectors to 50 to 100 microns and designing a more optimum support structure. At the present time, we envision two strategies to achieve such reductions. The first is to locate the output amplifiers and all of the input and output contact pads on one end of each CCD. The connections can thus be made on the outside ends of each two CCD ladder and there is no need for traces to run the full length of the ladders. The second is to eliminate the beryllium support layer and support each CCD ladder by stretching the CCD's from supports at each end of the ladder.

## 2 Relationship to Other Similar R&D Programs

- 2.1 Last year we submitted a proposal to the DOE Advanced Detector Research Program for R&D on CCD detectors and this proposal has been approved for one year of modest funding. In this first year we propose to remove the inactive SLD vertex detector VXD3 from SLD and make detailed measurements of the level and character of the radiation damage from three years of SLD data taking. In addition to normal running, at least once, early in the run, undamped beams were brought through the detector, exposing the CCDs to unusually large levels of radiation. The inner South CCDs were particularly affected as they face the beampipe. We also propose to expose some of these CCDs to increasingly larger doses of both ionizing radiation and to neutron fluxes in various test beams. This will allow us to study the effects of a range of radiation doses and thus measure the limits of radiation hardness for these devices and even more importantly, to characterize the failure modes. We expect ionizing radiation to create defects in the silicon dioxide and nitride dielectric, which increase the bias voltages required for satisfactory operation, and neutron fluxes to do bulk damage, creating charge traps.

A quantitative measurement of these effects will be very important in the design of detectors with improved radiation hardness. The observation of other unexpected failure modes would also be very important. Since we were in an extreme rush when VXD3 was built and installed (installation was completed within two years of project approval), these detailed studies were not carried out, so these studies should yield new information. This is a very cost effective and

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leveraged study since the CCDs, the readout electronics, and all the interconnections exist and thus a very modest investment of new R&D funds will yield important new information.

These studies will build on radiation damage studies that we have been conducting regarding the hardness to neutrons.\* Our measurements showed that neutron irradiation of vertex detector CCDs with a dose of a few times  $10^9$  n/cm<sup>2</sup> creates noticeable effects on the CCD charge transfer efficiency. However, this effect may be significantly reduced by the sacrificial charge technique. With the integration of the sacrificial charge technique into the CCDs, we estimated that the CCDs can operate efficiently up to and just beyond  $10^{10}$  n/cm<sup>2</sup>. The main contribution to the trapping defects in the neutron irradiated CCDs appeared to be from vacancy-phosphorus (VP) complexes. These measurements indicated that a CCD vertex detector probably can operate in the environment of a TeV energy linear collider, although development work was called for. A margin of safety is certainly desirable, since the estimates of neutron rates (and charge particle rates) could be low, by as much as an order of magnitude. In order to implement the sacrificial charge technique, CCDs with built in charge injection will need to be developed. In summary, the CCDs should be rad-hard enough for the NLC with the improvements we are planning.

- 2.2 There is a significant R&D effort on CCD vertex detectors in Europe led by Chris Damerell of Rutherford Labs. Our groups at Oregon and Yale have worked in close collaboration with Chris Damerell on the SLD Vertex Detector. We are at this time in close contact with the work of the European group and will carefully coordinate our activities with them to supplement, rather than duplicate, the R&D effort.
- a) We are planning to concentrate initially on developing CCDs for the NLC readout timing requirements. This is in any case a necessary first step toward the more demanding requirements for TESLA, should that be the ultimate technology for the future  $e^+ e^-$  collider. The European group will concentrate their efforts on the TESLA parameters, so that the activities of the two groups should complement each other.
  - b) In our R&D program, we propose to identify and start discussions with various commercial silicon fabrication houses to develop potential partners in the design and fabrication of CCDs for both the R&D prototypes and the final detector components. The CCDs for the SLD vertex detector were fabricated by the EEV Company in England. This company now is Marconi Applied Technologies. The European vertex detector R&D program of Chris Damerell, et. al, is mostly concentrating on working with Marconi in their CCD development. We believe that it is quite important to develop alternate sources for these devices for a variety of reasons:

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\*J.E. Brau and N. Sinev, "Operation of a CCD particle detector in the presence of bulk neutron damage," IEEE Trans. Nucl. Sci. 47, 1898 (2000). (<http://blueox.uoregon.edu/~jimbrau/talks/IEEE-99/ieee99.ps>)

- (i) Each silicon fabricator uses different proprietary technologies and procedures and has different design rules. It is not clear which fabricator will be successful in developing a satisfactory device or who will produce the best product.
- (ii) The fabrication of the final complement of CCDs will be quite expensive (order of millions of dollars or so). At the time of placing an order, it will be quite important to have several potential suppliers so that competitive bidding can help to keep the costs down.
- (iii) Silicon fabrication is quite a volatile business. Fabricators are often bought or sold (Fairchild became Loral became Martin Lockheed, EEV is now Marconi, etc.) and often make decisions to discontinue various product lines (such as CCDs). The risk of a single supplier deciding to unexpectedly drop out of CCD fabrication seems quite unattractive.

For these reasons, we feel that it is quite important to develop alternate silicon fabrication houses to work with us to design and fabricate the appropriate CCDs. In the course of the design and fabrication of the Yale QUEST CCDs, we have made a number of contacts and worked with several silicon fabricators. We propose to build on this base of experience and initiate discussions with several potential silicon fabricators about the design of the CCDs required for these vertex detectors.

- 2.3 In this proposal we are not planning to work directly on the readout electronics for CCD Vertex Detectors. We are aware of several groups proposing to work on the fast readout electronics required for these detectors. In particular, we have had discussions with the European CCD Vertex Detector group and the Oklahoma-Boston U-Fermilab groups who are proposing to work on electronics. We plan to coordinate our efforts closely with these groups so that together we develop a coherent detector with CCDs and the electronics appropriate to read them out.

### 3 Work Plan and Deliverables

We are proposing here an additional three-year R&D program to address the issues discussed above. We foresee the following activities:

- a) Work Plan Year 1
  - Simulation studies of the effects of detector thickness on the physics, and coordination with other groups doing simulations
  - Complete the study of effects of radiation damage
  - Mechanical Engineering study of support scheme
  - Continue discussions with CCD designers and silicon fabrication houses
  - Start detailed design of CCD's for NLC

## b) Work Plan for Year 2

- Complete detailed design for CCDs
- Buy masks for CCD fabrication
- Place order and start fabrication of CCD prototypes
- Continue support structure engineering design

## c) Work Plan for Year 3

- Complete prototype CCD fabrication
- Test performance of prototype CCD's
- Radiation test of prototype CCD's
- Complete preliminary support structure design

## d) Deliverables after the 3 Year R&amp;D Program

- Preliminary support structure design
- First prototype CCD devices
- Performance and radiation tests of prototype CCD devices

## 4 Budget Estimates

Item	Request in Units of \$1000		
	Year 1	Year 2	Year 3
Engineering, Technician, Shop Support and Supplies			
At Oregon	25	25	25
At Yale	25	25	25
Subcontracts			
CCD Design	0	25	0
Masks	0	25	0
CCD Fabrication	<u>0</u>	<u>50</u>	<u>100</u>
Yearly Totals	50	150	150

A detailed breakdown of the first year budget request is as follows:

## a) At the University of Oregon

Material and Supplies	\$ 3,600
Electronic Components	4,000
Cryogenic Equipment	4,000
Machine and Electronic Shops (80 hours at \$40/hr)	3,200
Travel	<u>5,000</u>
Total Direct	\$19,800
Indirect (26% of Direct)	<u>5,200</u>
Total	\$25,000

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## b) At Yale University

Material and Supplies	\$ 5,000
Engineering (200 hours at \$48/hr)	9,600
Technician (60 hours at \$45/hr)	2,700
Machine Shop (25 hours at \$48/hr)	1,200
Travel	<u>4,000</u>
Total Direct	\$22,500
Indirect 62.5% of Travel	<u>2,500</u>
Total	\$25,000

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## 4.2. Development and design of an LC ASIC for CCD readout and data reduction (UCLC)

### Vertex Detector

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Boston University  
Oklahoma

FY 2003: \$73,700

FY 2004: \$86,400

FY 2005: \$95,300

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# Proposal to the University Consortium for a Linear Collider

August 30, 2002

## Proposal Name

Development and design of an LC ASIC for CCD readout and data reduction

## Classification (accelerator/detector: subsystem)

Vertex Detector

## Personnel and Institution(s) requesting funding

Boston University, Physics Department: Ulrich Heintz (asst. professor)

University of Oklahoma at Norman, Department of Physics: Patrick Skubic (professor), Rusty Boyd (engineer)

## Collaborators

William Wester, Fermilab

## Contact Person

Patrick Skubic  
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## Project Overview

A high-resolution vertex detector is a crucial component of the detector for a future linear collider. An impact parameter resolution  $\sigma \approx 5\mu\text{m} \oplus 10\mu\text{m} \text{ GeV}/p \sin^{3/2} \theta$  is desired both in  $r - \phi$  and  $z$  for flavour tagging that identifies tracks coming from primary, secondary or tertiary vertices created by the decay of particles in an event [1]. Charge coupled devices (CCD) are the most established technology for large-scale pixel vertex detectors. The SLD experiment has successfully operated a 307 Mpixel CCD vertex detector [2]. The major challenges for a CCD based vertex detector at a future linear collider are in three areas:

- reducing the amount of material by thinning the substrate;
- improving radiation hardness;
- increasing the readout speed.

This proposal will address the third challenge - readout speed. We propose to develop a readout system that will demonstrate the feasibility of use of CCD's at the LC, and could lead to designs for specific experiments. Other technologies that potentially have resolutions competitive with CCD's may also be investigated. We will collaborate with groups in the US and Europe that are developing CCD detectors for the LC. We will readout the CCD's being studied the the Oregon/Yale group, and those under

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development for Tesla by the Linear Collider Flavor Identification (LCFI) Collaboration in Europe. Some discussion with both groups has been started.

For the vertex detector of the SLD experiment, VXD3, there were 307 million CCD pixels[2]. The electronic circuitry that was used to handle this large number of pixels was complicated, involving at least 8 to 10 FPGA chips that were on FASTBUS modules. Readout of the SLD vertex detector took about 200 ms. For a linear collider application this time must be reduced by three orders of magnitude. To be able to read out the LC vertex detector it will be necessary to suppress pedestals on detector and replace some (or all) of the FASTBUS module functionality with much smaller and faster circuits, possibly contained in a single chip. A parallel readout architecture will have to be implemented.

We propose an R&D program that starts with the detailed study of the present VXD3 design developed at SLAC, and other pixel detectors to understand them thoroughly and will work in collaboration with Fermilab to develop ASIC's with improved performance. The proposed work would lead to the design of a highly efficient system, which can be used to improve the electronic performance and hence the accuracy of the detector. In order to test our chips, we propose developing a DAQ test station suitable for detector and readout bench/beam tests.

This effort builds upon previous VLSI work at University of Oklahoma. Five EE Masters students completed theses on VLSI related projects as members of our group. This includes the complete design, fabrication and testing at OU of 4 generations of a mixed-mode analog multiplexer IC, the VAMUX, which was used in the CLEO III, silicon sensor QA system. Three students contributed to the development of the ATLAS pixel detector front-end readout chip, in collaboration with LBNL. We have educational licenses for Cadence and other design tools.

We have had considerable experience with Maxwell Spicelink, which is a software package which can be used to extract the L, C and R parameters of metal traces and their electromagnetic interactions with surrounding materials, such as Si and dielectrics. Maxwell creates a Spice model of the circuitry from a 3-D drawing by solving the field equations using finite element analysis. This spice model can then be used in circuit simulations. These simulations would be very useful in evaluating designs of CCD's that can be read out at very high speeds, such as proposed for Tesla.

Boston University has previous experience with irradiation tests, design, and construction of the silicon strip detector for DØ and high-speed digital electronics for the level 2 silicon track trigger for DØ. We will draw on the Electronics Design Facility at Boston University [5] as a resource, which has extensive experience in FPGA design (DØ, CMS) and ASIC design (ATLAS). The facility also provides access to the advanced design tools required, such as Mentor and Cadence.

### **FY2003 Project Activities and Deliverables**

Presently, the VXD3 layout consists of three barrels with a total of 96 CCDs on 48 ladders with 4 outputs per CCD yielding a total of 384 outputs. These analogue outputs are digitized and applied with a clocking signal and a bias supply at the front-end (F/E) electronics whereas the FASTBUS modules are used for managing data acquisition and providing timing and control functions. The FASTBUS data acquisition modules are placed at a distance of 50 m from the F/E boards and are connected by optical fibers. For the SLD vertex detector, disruptions in the data link occurred during accelerator operation. For reduction in the amount of devices used and to make the circuit smaller for subsequent improvement in the data processing speed and reliability, we would like to develop a new design. Replacing FASTBUS module functionality with smaller chips will enable us to place them on the barrel itself, close to the F/E hybrids. This will also make it inaccessible after detector installation, so it has to be completely reliable and able to withstand the radiation environment.

The objective for the first year would be to develop a set of specifications for the ASIC such as modularity, number of gates required for the entire operation and the identification of the design methods and development tools that are appropriate for this project. We will study the use of ASIC's and FPGA's to optimize the design for the LC. The specifications will be developed in close coordination with the Oregon/Yale and LCFI groups working on CCD detector development. We also anticipate fabrication of a small number of test structures through MOSIS in the first year. This would mainly be done by Oklahoma and Fermilab.

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In order to test prototype vertex detector elements and/or readout chips a simple data acquisition system is required, that can be operated with minimal infrastructure requirements. The Fermilab Computing Division ESE Group has developed a general purpose set of PCI Test Adapter Cards for the BTeV experiment [3,4] that will form the basis of the BTeV pixel detector test stands. These cards are also used to test the SVX4 readout chip for the silicon strip detectors for CDF and DØ. These cards feature large FPGAs that can be programmed to interact with the device to be tested. It seems that these boards could be very useful for linear collider vertex detector test stands as well. This would mainly be done by the Boston group.

We propose to obtain a few sets of these boards and assemble a test DAQ system, using a PC provided by Boston University. We will understand the capability of the system and learn how to program it. By the end of the first year we intend to have the system running in a sample data acquisition application. This may require the design of an additional interface card for the specific detector. This project is well suited in scope for a graduate student.

### **FY2004 Project Activities and Deliverables**

During the second year the engineers at all three institutions will collaborate in the development of a prototype readout chip for CCDs, following the specifications that were developed in the first year. We intend to use the DAQ system developed in the first year to test these prototype devices.

### **FY2005 Project Activities and Deliverables**

During the third year the design of the readout chip will be finalized using the experience gained from the prototype tests during the previous year. The ultimate goal is to obtain a functional design for a readout chip that establishes the technical feasibility and can serve as the starting point for a production design.

references:

- 1 J.Brau et al., "Linear Collider R&D" (<http://blueox.uoregon.edu/~jimbrau/LC/LCrandd.ps>).
- 2 K. Abe, et al., "Design and Performance of the SLD vertex detector: a 307 Mpixel tracking system", Nucl. Instru. and Meth. A400 (1997) 287-343.
- 3 K. Treptow, G. Deuerling, "PCI Test Adapter Card" ([http://www-ese.fnal.gov/eseproj/BTeV/TestStands/PCI\\_Test\\_Adapter.doc](http://www-ese.fnal.gov/eseproj/BTeV/TestStands/PCI_Test_Adapter.doc)).
- 4 J. Andresen et al., "Programmable Mezzanine Card (PMC)" ([http://www-ese.fnal.gov/eseproj/BTeV/TestStands/PMC/Prgm\\_MezzanineCard.pdf](http://www-ese.fnal.gov/eseproj/BTeV/TestStands/PMC/Prgm_MezzanineCard.pdf)).
- 5 see web page at <http://ohm.bu.edu/edf.html>.

### **Budget justification**

Boston University: We ask for support for a graduate student, who will work 90% on this project during the first year. During the second and third year the student will be 50% on DØ, doing his thesis research and 50% on this project, which will provide the hardware experience that is a crucial part of graduate education in particle physics. The graduate student is charged at the rate for graduate assistantships set by the BU College of Arts and Sciences for FY 2002 (\$1812.5/month), increased by an estimated 5% per year thereafter. We are also asking for support for 20% of an electrical engineer starting in the second year at the current subsidized EDF rate of \$35/hour (in the other direct costs category). We request travel support for about two trips each in years 1 and 2, and four trips in year 3 to Fermilab or other collaborating institutions for meetings. Indirect costs are calculated at BU's rate of 63%. The equipment budget includes one set of PCI Test Adapter boards (\$2000/set) and funds for an interface card (\$2500) in the first year and \$2500 in the second and third years for fabrication of readout chip prototypes.

University of Oklahoma: We request a modest amount of support to fund an Electrical Engineering Graduate Research Assistant. (A small tuition remission fee is listed under other direct costs.) An EE graduate student, P. Kshirsagar, has been involved in development of this proposal and would like to

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use this project as the basis for her thesis. Our electronics engineer, G. Boyd, who is supported by our operating grant, will also participate in the design, fabrication and testing for this project. Fermilab will contribute to the design effort. We are requesting equipment funds each year for chip fabrication through MOSIS and readout electronics to support development. We request travel funds to allow us to make six round trips per year to Fermilab for meetings with collaborating physicists and engineers from Fermilab and BU. Indirect costs are calculated using the OU rate of 45.5% excluding equipment.

**Three-year budget, in then-year K\$****Institution:** Boston University

Item	FY2003	FY2004	FY2005	Total
Other Professionals	0	0	0	0
Graduate Students	\$20.5k	\$12.0k	\$12.6k	\$45.1k
Undergraduate Students	0	0	0	0
Total Salaries and Wages	\$20.5k	\$12.0k	\$12.6k	\$45.1k
Fringe Benefits	0	0	0	0
Total Salaries, Wages and Fringe Benefits	\$20.5k	\$12.0k	\$12.6k	\$45.1k
Equipment	0	0	0	0
Travel	\$1.2k	\$1.2k	\$2.4k	\$4.8k
Materials and Supplies	\$4.5k	\$2.5k	2.5k	\$9.5k
Other direct costs	0	\$14.0k	\$14.0k	\$28.0k
Total direct costs	\$26.2k	\$29.7k	\$31.5k	\$87.4k
Indirect costs	\$16.5k	\$18.7k	\$19.8k	\$55.1k
Total direct and indirect costs	\$42.7k	\$48.4k	\$51.3k	\$142.5k

**Institution:** University of Oklahoma

Item	FY2003	FY2004	FY2005	Total
Other Professionals	0	0	0	0
Graduate Students	\$12k	\$13k	\$14k	\$39k
Undergraduate Students	0	0	0	0
Total Salaries and Wages	\$12k	\$13k	\$14k	\$39k
Fringe Benefits	\$1k	\$1k	\$1k	\$3k
Total Salaries, Wages and Fringe Benefits	\$13k	\$14k	\$15k	\$42k
Equipment	\$5k	\$10k	\$15k	\$30k
Travel	\$4k	\$4k	\$4k	\$12k
Materials and Supplies	0	0	0	0
Other direct costs	\$1k	\$1k	\$1k	\$3k
Total direct costs	\$23k	\$29k	\$35k	\$87k
Indirect costs	\$8k	\$9k	\$9k	\$26k
Total direct and indirect costs	\$31k	\$38k	\$44k	\$113k

## 4.3. Study of the Mechanical Behavior of Thin silicon and the Development of hybrid silicon pixels for the LC (UCLC)

### Vertex Detector

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Purdue

FY 2003: \$39,350  
FY 2004: \$40,000  
FY 2005: \$153,250

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## 1. Project Name: Study of the Mechanical Behavior of Thin silicon and the Development of hybrid silicon pixels for the LC

### Classification (accelerator/detector subsystem)

Detector: tracking and vertex

### Institution(s) and personnel

Purdue University: Daniela Bortoletto, Ian Shipsey

### Collaborators

FERMILAB: Simon Kwan, Jim Fast, Cristian Gingu, William Wester

### Contact Person

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## 2. Project overview

The scope of this project is twofold. The first goal is to increase our understanding of the mechanical stability of thin silicon. Second we would like to understand the physics reach of a thin hybrid pixel system at a linear collider. The mechanical studies will have an impact not only for hybrid pixels but also for CCD, silicon microstrip detectors and other attractive thin substrate technologies such as MAPS (Monolithic Active Pixels Sensors).

Physics studies have shown the jet flavor identification with high efficiency and purity is a critical element in the full exploitation of the physics potential of the Linear Collider (LC). Jet flavor identification can be achieved in the highly collimated jets expected at the LC with precise vertex detection based on pixel detector technology achieving an impact parameter resolution of  $5\mu\text{m} \oplus 15\mu\text{m}/p_t(\text{GeV}/c)$  or better. In this expression the first term depends on the detector intrinsic single point resolution and geometry while the second term accounts for multiple scattering. The impact resolution requirements translate into a single point resolution of  $7\mu\text{m}$  and a material budget of  $0.5\% X_0$  for each layer in an n layer device.

The Charged Coupled Devices (CCD) operating at the SLD have demonstrated a resolution and a thickness close to the requirements. Improvements are needed to achieve the readout speed required for operation at future machines such as TESLA where the single bunch crossing will occur every 330 ns. Another areas of concern is the radiation tolerance of a CCD and studies are taking place to evaluate the radiation damage of the SLD CCDs.

Several studies have taken place in Europe that investigate an alternative approach to jet flavor identification based on solid-state hybrid detectors. Hybrid pixel detectors will be used as vertex detectors for the CMS and Atlas experiments. They have the advantage of fast time stamping, sparse data read out, and excellent radiation tolerance. Research and

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Development are required for possible application of this technology to the LC in the following areas: (1) improvement in the point resolution, which is currently limited by the pixel dimensions of  $50\ \mu\text{m} \times 300\ \mu\text{m}$  (2) reduction in material. The standard thickness in silicon processing is  $270\ \mu\text{m}$ .

Better resolution can be achieved by adopting an interleaved pixel read out as shown in [1]. This approach is similar to charge sharing through capacitive coupling in silicon strip using intermediate strips [2] and it has already produced interesting results. Moreover since this R&D was started in Europe, several advances have taken place such as the development of  $0.25\ \mu\text{m}$  technology that should allow the hybrid technology to achieve a smaller cell dimension.

A reduction in material can be achieved directly by fabricating thin silicon sensors and read-out, or by thinning the substrates after processing. The Atlas and the BTeV collaborations have already performed extensive R&D on thinning techniques for hadron colliders applications. Since the voltage required to fully deplete a silicon sensor is proportional to the detector thickness squared, a reduction by a factor of 2 in the thickness implies a factor of 4 in the required operating voltage at any given integrated fluence with clear beneficial implications for the lifetime of the detector itself.

The project is a collaboration between Fermilab and Purdue University. The group at Purdue University has already received funding through the DOE ADR program to study thin silicon sensor production. The proposed effort builds upon our experience in design and testing of silicon micro-strip and silicon pixels for CDF and CMS. We have access to CADENCE design tools and DESSIS simulation tools. The mechanical aspects of the project building upon our experience in the mechanical design, fabrication, and assembly of the silicon detector for CLEO III, and the mechanical design and prototyping of parts of the CMS forward pixel detector.

The detector facility at Purdue University contains two fully equipped clean rooms for the design, testing and assembly of detectors for High Energy Physics. These clean rooms are part of a complex dedicated to microstructure detector development and fabrication including silicon strip and pixel devices and micro pattern gas detectors. The total clean room space is 3000 sq ft in three laboratories containing a CMM, wirebonder, electrical testing equipment, probe stations, optical tables, microscopes and high precision measuring devices. The labs are fully equipped with computer facilities for control, data acquisition and analysis. The labs have both temperature and humidity control and HEPA filtering of the airflow. Included in the clean rooms is additional space of class 1000. In a separate location there is a detector irradiation facility with an X-ray source and an ultra clean gas delivery system used for the development and testing of micro pattern gas detectors.

Other technical resources are also available, such as machine and electronic shops within the physics department, a central machine shop and state of the art facilities on campus, such as SEM, TEM (Transmission Electron Microscopy) and EDS (Energy Dispersive Spectroscopy). In addition to the technical staff, an engineer and technician, there is the

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normal complement of graduate students and research associates working on specific projects. There is also an exceptional pool of talented undergraduates who work on R&D and detector construction projects

References:

- [1] M. Battaglia et al., IEEE Nuclear Science Symposium and Medical Imaging Conference, October 15-20, 2000, Lyon, France, IEEE Trans.Nucl.Sci. 48 (2001) 992-996; M. Battaglia et al., Proceedings of the 9th Int. Workshop on Vertex Detectors, Lake Michigan MI (USA), September 2000, Nucl.Instrum.Meth. A473 (2001) 79-82.
- [2] A Piesert, in Instrumentation in High Energy Physics, New York, World Scientific, 1, 1992

### 3. Project Activities and Deliverables

#### 3.1 FY2003

Several activities to study the mechanical stability of thin silicon and determine if the hybrid technology is a viable solution are planned for the first year:

- 1) Verification that the requirement  $5\mu\text{m} \oplus 15\mu\text{m} / p_t(\text{GeV}/c)$  is correct in collaboration with the LC tracking and vertexing simulation group. Simulation of the optimal interleaved pixel layout to achieve the needed single point resolution of  $7\mu\text{m}$ . Establish target thickness for layers of hybrid pixel devices at different distances from the interaction point. The optimization process will be carried out by studying the effect of the layer thickness on the flavor tagging efficiency and purity. This is a crucial element to determine the Higgs branching fractions.
- 2) Studies with vendors of the minimum thickness that can be achieved in single sided pixel manufacturing. This will use ADR funding.
- 3) The Fermilab group will lead in studies of thinning the ROC and silicon sensors by continuing and expanding the R&D that is already taking place within BTeV. Blank silicon samples will also be used.
- 4) Produce prototypes with interleaved sensors and ROC already available, monitor their behavior, and build a measurement fixture for mechanical studies. These studies will be conducted with the readout chip designed for the BTeV detector which is designed for n on n sensors since in high intensity proton machines space charge inversion will be reached after a few months of running.
- 5) Studies of alignment and fabrication of low mass support frames. Metrology will be performed during cooling cycles. These will need to be conducted at cryogenic temperatures for CCD application. Finite Element Analysis (FEA) will be also performed to understand the mechanical stability of the thin silicon.

The first year deliverable will be an initial determination of the potential of hybrid technology for the LC. We will also study systematically the stability issues associated with thin silicon.

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### **3.2 FY2004**

In the second year we will continue the mechanical studies of the initial prototypes. Systematic studies will also be performed to determine the resolution and charge collection efficiency with cosmic rays, diodes, and possibly beam tests. Comparison of MC simulations with the performance of interleaved n on n pixels readout with the BTeV chip.

This will allow a first evaluation of the potential gain in resolution that can be achieved with thin and interleaved hybrid sensors.

### **3.3 FY2005**

Based on the results of FY2003 and FY2004, we plan to start the production of thinner sensors with the optimal interleaved LC layout. This will require masks and fabrication funding. We will also need a readout chip to match the p on n sensor for the LC. The chip designers could use the latest chip technology that will be available at that point to minimize pixel size.

The third year deliverables will be thin interleaved sensors designed to achieve the intrinsic point resolution needed at the LC and an optimal chip for the LC. This will allow a realistic assessment of the viability of the hybrid technology for the LC.

## **4. Budget Justification**

### **4.1 First Year Budget**

The first year equipment budget will allow Fermilab to build a system to study the mechanical issues connected with the thinning of sensors and readout chips. The study will include precision measurement of the stability of the support schemes including temperature cycles. Some of these studies will be conducted with blank silicon and some with BTeV prototypes. Fermilab will provide personnel to perform finite element analysis (FEA) studies. The personnel will be supported with Fermilab funding.

The graduate student at Purdue will start device simulation and MC studies to understand the optimal interleaved sensors layout for the LC. Thin sensors provided by the ADR funding will allow a determination of the yield and the minimum thickness that is achievable by the vendors.

#### **Equipment breakdown:**

##### **1) Precision alignment tooling: \$1.5K**

Vacuum holders for sensor/ROC assemblies and holder for support frame that precisely aligns the modules to the support frames. Cost is based on recent experience with similar tooling for Run IIb R&D efforts.

##### **2) Adhesives: 0.4K**

Adhesives for attachment of modules to supports. Cost is based on recent purchases of adhesives in minimum quantities for Run IIb R&D.

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**3) Engineering analysis (FEA): (1.5 K at no cost - supported by Fermilab)**

This allows for 30 hours of engineering analysis by the FNAL analysis group.

**4) Fabrication and assembly of a low-mass support frame: \$2.7K**

Support frame will be either beryllium or carbon composite and will need to be of reasonably high precision.

**5) Thinned silicon, 2 batches @ \$1K per batch: \$2K**

Cost estimate is based on previous purchases.

**6) Metrology, assuming we draw on available infrastructure from BTeV: \$2.0K**

This involves modifications to allow us to mount our samples in a dry chamber at low temperature in order to be optically inspected through a window. BTeV has already built the chamber itself for their pixel studies. We will need to provide mounting and cooling connections to our samples. In particular we will need to go to much lower temperatures than BTeV. Modifications to allow for operation at cryogenic temperature dominate this cost.

The travel request includes 2K for Purdue to visit companies and attend LC meetings

**4.2 Second Year Budget**

The second year requires support for a cosmic ray setup and beam tests with interleaved pixel prototype matching the BTeV chip. The travel request includes 2K for Purdue to visit companies and attend LC meetings.

**4.3 Third Year Budget**

The third year budget is for the production of hybrid-pixel specific for LC development. This requires funding for prototype sensors and readout chip. This is necessary since most of the development for ATLAS, CMS and BTeV is based on n on n sensors while at the LC single sided p on n sensors could be more cost effective since the radiation level at the LC is less challenging. The travel request includes 2K for Purdue to visit companies and attend LC meetings.

**4.4 Three-Year Budget in then-year K\$**

**Institution:** Purdue University

Item	FY2003	FY2004	FY2005	Total
Graduate student	23	24	25	72
Equipment	8.6	8	120	136.6
Travel	2	2	2	6
Total direct costs	33.6	34	147	214.6
Indirect Costs	5.75	6	6.25	18
Total	39.35	40	153.25	232.6

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## 4.4. Investigation of new technologies for the silicon vertex tracker (LCRD)

### Vertex Detector

Contact person: David Buchholz  
email: dbuchholz@nwu.edu  
phone: (847) 491 5454

Fermilab  
Northwestern

FY 2003: \$23,000

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**Project name**

Investigation of new technologies for the silicon vertex tracker

**Classification (accelerator/detector:subsystem)**

Detector: Vertex Detector

**Institution(s) and personnel**

Northwestern University, Department of Physics and Astronomy:

David Buchholz (professor), Harald Fox (postdoc)

Fermi National Accelerator Laboratory:

Ron Lipton (staff scientist), William Wester (staff scientist), Simon Kwan (staff scientist)

**Contact person**

David Buchholz

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(847) 491 5454

**Project Overview**

The vertex detector for the linear collider needs to have high resolution impact parameter measurement in order to achieve the goals of the proposed physics program. The present design of the vertex detector is based on pixelated silicon detectors. These detectors achieve excellent position resolution. Several concepts are under investigation for the future linear collider. Among them are:

- A detector based on Charged Coupled Devices (CCD). The SLD collaboration already successfully employed CCD technology. This detector has proven to have a very good spatial resolution and offers the possibility to use thin silicon sensors. On the down side of this technology is the limited radiation hardness and the necessity for cooling of the devices. The radiation hardness is a problem that may exclude this technology. R&D for this detector type is performed by several collaborations in the UK, US and Japan.
- Monolithic Active Pixel Sensors (MAPS) based on CMOS technology is a new development pursued in France and the UK. The main advantage is that industry standard VLSI technology can be used. This can reduce the cost of the vertex detector considerably. It also offers the possibility to integrate readout functionality into the pixel itself. It is envisaged to develop thin silicon sensors in this technology to suit the need of a linear collider detector. A prototype version of a MAPS detector using a 64x64 pixel matrix exists.
- A collaboration in Germany uses an array of Depleted Field Effect Transistors (DEPFET) as sensor. This detector type has an excellent noise performance as the first amplification stage is already integrated into the pixel. DEPFET pixels also have very low power consumption as they are only active during readout. Both features make it possible to operate a DEPFET

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vertex detector at room temperature eliminating the need for extensive cooling. A 64x64 pixel prototype detector has been operated routinely using low energy photon sources. The development of a thinned detector is well under way.

These three detector options offer exciting prospects for the future. We are in contact with those collaborations to explore possible contributions to the ongoing R&D effort. While we will concentrate on the US based CCD R&D effort we do not want exclude looking at other different detector options. Three main areas of R&D are:

- The neutron flux from accelerator background is expected to be about  $10^9/\text{cm}^2/\text{year}$ . Additional background comes from electron-positron pairs. The silicon detectors must survive this flux for many years.
- The intrinsically high number of channels of pixelated detectors poses a challenge to the readout. A readout cycle of the inner detectors must be completed within  $50\mu\text{s}$ .
- The detector thickness should be as thin as possible to avoid degradation of the momentum resolution by multiple scattering.

The proximity to Fermilab offers the possibility to address those problems. The members of this proposal have experience with building the DØ (Lipton, Buchholz, Fox) and the CDF (Wester) vertex detectors. Some of us (Wester and Kwan) are also involved in R&D for the BTeV vertex detector.

In the past the Fermilab booster facility has been used to irradiate silicon detectors for DØ and CDF. Additional radiation tests are planned for the Run IIb upgrade of both detectors. We also have experience with irradiation of silicon detectors with Cobalt-60 and neutron sources. In addition some of us worked on the readout of silicon detectors (Wester, Buchholz, Fox) and on thinning silicon detectors for the BTeV experiment (Kwan).

### **Description of first year project activities**

We propose to use the opportunities that the R&D for DØ, CDF and BTeV detectors offer for silicon detectors for the linear collider vertex detector R&D.

- The Fermilab Computing Division has developed a generic readout system for the BTeV experiment. The readout utilizes the commercial PCI bus. A PCI Test Adapter Card (PTA) is used together with a PC. The PTA card hosts a Programmable Mezzanine Card (PMC). These cards feature large FPGAs and memory components. They provide a large number of freely programmable input and output channels that can work with a wide variety of readout chips. This system is used for the BTeV test stand. Work is underway to use it also for the DØ and CDF SVX4 readout chip. We propose to adapt this system to the readout chip used on a prototype sensor. This enables us to read out the silicon sensor without having to develop custom designed hardware components first. This setup is a cost effective and easy to use solution for all test stands where readout is required. We are aware that our DØ collaborator Ulrich Heintz from Boston University wants to use this system for R&D on ASIC readout chips. We plan to closely work together with him.

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- We propose to use the Fermilab booster and other facilities to irradiate prototype detectors. Together with the readout system described above the effect of radiation damage on the detector performance can be estimated. These studies will help the group working on the silicon sensor design to evaluate their prototype detectors and to optimize radiation hardness.
- At a later stage we plan to use the Fermilab booster facility for further beam studies. We propose to build a beam telescope using the readout system described above. This would allow us to measure detection efficiency and detector resolution directly with a m.i.p. beam. This will help the group designing the silicon sensor to evaluate and optimize prototype detectors.

This project is ideal for participation of a student at various stages of the project. We are therefore requesting funding for one undergraduate student majoring in physics. We also ask for a modest amount of travel money to be able to go to linear collider related meetings and to travel to irradiation sites.

### Budget

Institution	Item	Cost
Northwestern	PC based readout system (PC, PTA, PCM, Software)	\$ 6,000
Northwestern	Silicon fixture	\$ 5,000
Northwestern	Summer + academic year salary for one undergraduate student	\$ 4,415
Northwestern	Fringe benefits for above	\$ 839
Northwestern	Travel costs	\$ 2,000
Northwestern	Indirect cost at 26% off campus rate	\$ 4,746
	Grand total	\$23,000