

# Vertex Detector

## Vertex Detector Table of Contents

Table of Contents and Overview .....	4.0
40. Pixel Vertex Detector R&D for Future High Energy Linear e+ e- Colliders (LCRD; Charlie Baltay) .....	4.1
41. Development and design of an LC ASIC for CCD readout and data reduction (UCLC; Patrick Skubic) .....	4.2
42. Study of the Mechanical Behavior of Thin silicon and the Development of hybrid silicon pixels for the LC (UCLC; Daniella Bortoletto) .....	4.3

### Vertex Detector Proposals Overview

The Vertex Tracker has to provide the jet flavour identification and accurate track reconstruction that are prerequisites to most if not all of the linear collider physics program. In some detector concepts, the vertex detector takes on an added role of charged particle pattern recognition as well. If the Higgs boson exists and is light, as the data collected so far indicate, its couplings to fermions of different flavour and mass must be accurately measured to test the Higgs mechanism of mass generation. Efficient flavor tagging in multi-jet events and determination of heavy quark charge will be instrumental to study signals of New Physics both through the direct production of new heavy particles, coupled predominantly to b and t quarks, and through precision measurements of electroweak processes at the highest energies. Physics requirements push the vertex tracker specifications to new levels. While much has been learned in two decades of R&D on Si detectors for the LHC experiments, the linear collider requirements motivate new and complementary directions for detector development. The linear collider environment, with its lower event rates and lower radiation, admits Si sensors that are substantially thinner, more precise and more segmented than at the LHC. Technologies which have not been applicable in the high radiation environment of proton colliders are available, as well as sensors based on new concepts. Significant R&D is required to solve the detector problems of the LC environment. CCD vertex detectors have already demonstrated very high resolution and segmentation with moderate multiple scattering. But for the CCD technology to be applicable to the LC improved radiation hardness and a factor 100-1000 increase in readout speed are required. Technologies successfully developed for the LHC program, such as hybrid pixel sensors, are sufficiently radiation hard and can be read out rapidly. But they now need to be developed into much thinner devices with smaller cell size to improve their tracking resolution capabilities. Finally new technologies, such as CMOS sensors, have emerged as potentially attractive solutions. But they need to be demonstrated on large scales and be tailored to the linear collider application. These developments need to be guided by a continuing program of physics studies and detailed simulations to define the optimal designs and technology choices.

The three proposals submitted and detailed below address these outstanding R&D issues following all three paths discussed above. The Oregon/Yale (A) and Boston University/Oklahoma/FNAL (B) proposals focus on CCD technology. They address the improvement of the radiation hardness, the development of new, faster and thinner CCD sensors and the design of advanced CCD readout schemes. Evaluation of CMOS sensors as a viable alternative to CCD sensors will also be considered within the Oregon/Yale proposal. The Purdue/FNAL (C) proposal considers further evolutions of the hybrid pixel concept to develop thinner devices, providing higher spatial resolution. As a significant effort on Si detector R&D is ongoing in Europe and also in Asia, these efforts make provisions for coordinated activities and sharing of experience which ensure mutual benefits in the design of the linear collider detector.

A.	LCRD 4.1	Pixel Vertex Detector R&D for Future High Energy Linear e+ e- Colliders	Jim Brau Charley Baltay	U. Oregon Yale U.
B.	UCLC 4.2	Development and design of an LC ASIC for CCD readout and data reduction	P. Skubic	U.Oklahoma Boston U.
C.	UCLC 4.3	Study of the Mechanical Behavior of Thin silicon and the Development of hybrid silicon pixels for the LC	D. Bortoletto	Purdue U.

## 4.1. Pixel Vertex Detector R&D for Future High Energy Linear e<sup>+</sup> e<sup>-</sup> Colliders (LCRD)

### Vertex Detector

Contact person: Charlie Baltay  
email: [baltay@yale2.physics.yale.edu](mailto:baltay@yale2.physics.yale.edu)  
phone: (203) 432-3386

Oregon  
Yale  
Oklahoma  
SLAC  
Rutherford Lab  
KEK  
FNAL

Year 1: \$75,000  
Year 2: \$150,000  
Year 3: \$150,000

# Pixel Vertex Detector R&D for Future High Energy Linear $e^+ e^-$ Colliders

J. Brau, O. Igonkina, N. Sinev, D. Strom      University of Oregon

C. Baltay, W. Emmet, H. Neal, D. Rabinowitz      Yale University

Research is coordinated with: M Breidenbach, SLAC; A. Miyamoto, Y. Sugimoto, KEK;  
P. Skubic, U. of Oklahoma; R. Yarema, W. Wester, FNAL;  
C. Damerell and the LCFI, Rutherford Lab.

## 1. Introduction

Studies carried out in the U.S., Europe, and Asia, have demonstrated the power of a pixel vertex detector in physics investigations at a future high energy linear collider. Many factors suggest the most attractive technology is silicon charge coupled devices (CCDs). Other technologies being considered include CMOS pixels<sup>1</sup>, DEPFETs<sup>2</sup>, and hybrid pixels under development for LHC detectors. CCD have the advantage of small pixels for superior spatial resolution and the possibility of very thin detector layers to minimize multiple scattering which is the factor limiting the resolution of the interesting lower momenta. They are also the most mature of the technologies being considered, having successfully been used in the 307 Mpixel vertex detector of SLD, VXD3.<sup>3</sup> However, other approaches, such as the CMOS pixels, offer similar advantages, if they can be realized in the large systems already demonstrated by CCDs, and have the potential of significantly faster read out capability.

## 2. Objectives of the Proposed Project

### 2.1 Development of CCD Detectors

Despite the advantages of CCDs for the vertex detector at the next generation linear collider, there are significant questions about their feasibility. These are principally the radiation tolerance, the readout speed, and, to a less degree, the mechanical structure. This proposal is focused on addressing these major issues, and beginning an investigation into the feasibility of CMOS pixels.

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<sup>1</sup> Institut de Recherches Subatomiques, Strasbourg, France,  
<http://ireswww.in2p3.fr/ires/recherche/capteurs/>; Rutherford Appleton Laboratory,  
[http://www.te.rl.ac.uk/med/projects/High\\_Energy\\_Physics/R+D/MAPS/proj.htm](http://www.te.rl.ac.uk/med/projects/High_Energy_Physics/R+D/MAPS/proj.htm)

<sup>2</sup> The DEpleted P-channel Field Effect Transistor(DEPFET),  
<http://www.hll.mpg.de/depfet/>

<sup>3</sup> K. Abe et al, "Design and Performance of the SLD Vertex Detector, A 307 Mpixel Tracking System", Nucl.Instrum.Meth.A400:287-343,1997 .

### 2.1.1. Increasing the Radiation Hardness of CCD

The expected radiation dose at the SLC was less than 1 krad for the lifetime of the SLD vertex detector and the CCD were tested to operate at a dose of 10 krad. The detailed background calculations for the next generation  $e^+ e^-$  colliders indicate an upper limit of 100 krad/10 years, a factor of 100 to 1000 higher than at the SLC. The neutron backgrounds are estimated to be  $\sim 10^9$  neutrons/cm<sup>2</sup>/year, larger than at the SLC by a similar factor. We believe that this increase in radiation tolerance can be achieved by various strategies. Reducing the thickness of the surface silicon dioxide layer will reduce the surface damage from ionizing radiation, and reducing the well size in the pixels will reduce the amount of bulk damage. Furthermore, the use of the sacrificial charge technique will reduce the effect of bulk damage on the charge transfer efficiency. To test the success of these strategies will require the design of new CCD, the fabrication of these devices by commercial silicon fabrication houses, and radiation testing the resulting CCD.

### 2.1.2. Decreasing the CCD Readout Time

For the NLC the CCDs have to be read out in the 8.3 msec interval between trains of 190 bunches spaced at 1.4 ns. (The GLC has very similar requirements, so when we refer to NLC, it should be understood also to refer to the GLC.) For TESLA occupancy from a full 2820 bunch train is too large, requiring that partial read out to occur between the 337 ns interval between bunches in the train. This has led to the column parallel readout development effort by the LCFI, when each column has its own readout node.<sup>4</sup> For NLC we imagine increasing the readout rates to 25-50 MHz (the SLD vertex detector was read out at 5 MHz) and increasing the number of readout nodes to 20 to 40 per CCDs. We believe that this scheme is achievable, but it will require a new CCD design and a prototype CCD fabrication run to test the new design. To achieve the same performance at TESLA, another factor of about 100 would be needed in the product of readout nodes and readout rate.

### 2.1.3 Reducing the CCD and the Support Structure Thickness

A large fraction of the particles of interest at the linear collider are of such low momentum that their measurements are significantly affected by multiple scattering. This motivates reduction of the layers of the vertex to 0.1 to 0.2% of a radiation length, which requires reducing the thickness of the CCD detectors to 50 to 100 microns and designing a more optimum support structure. At the present time, we envision two strategies to achieve such reductions. The first is to locate the output amplifiers and all

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<sup>4</sup> Linear Collider Flavour Identification Collaboration, <http://hepwww.rl.ac.uk/lcfi>

of the input and output contact pads on one end of each CCD. The connections can thus be made on the outside ends of each two CCD ladder and there is no need for traces to run the full length of the ladders. The second is to eliminate or substantially reduce the beryllium support layer and support each CCD ladder by stretching the CCD from supports at each end of the ladder.

## 2.2 Investigation of CMOS pixels

A very attractive alternative to CCDs is offered by the CMOS pixel technology. Like CCDs, this technology takes advantage of a large industrial interest for other applications. It's advantages relative to CCDs include:

1. Significantly faster read out due to the capability of these devices to read out the x,y coordinates of only the pixels that have a hit in them.
2. Potentially more rad-hard operation
3. Simpler fabrication and operation

It's challenges include:

1. Power budget
2. Maintaining good signal/noise (where signal is very small)
3. Large scale readout
4. Large system performance
5. Reducing thickness

## 3. Progress through November, 2003

Our progress has been reported in a number of talks recently.<sup>5</sup> We summarize here this progress.

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<sup>5</sup> J. E. Brau, "Studies of radiation damage to vertex detector CCDs," ECFA-DESY Linear Collider Workshop, Amsterdam, April, 2003, <http://www.nikhef.nl/ecfa-desy/ECspecific/Program/Presentations/April-2/Par-3/3A/brau-j.ppt>;  
O. Igonkina, "CCD Radiation Damage Studies," Cornell Linear Collider Workshop, July, 2003, <http://blueox.uoregon.edu/~lc/cornell-vxd/igonkina.pdf>;  
N. Sinev, "Investigation of Effects in the Neutron and Electron Irradiated CCD," Vertex 2003 Workshop, Lake Windermere, UK, September, 2003, <http://hepwww.rl.ac.uk/Vertex03/Talks/NikolaiSinev.pdf>;  
N. Sinev, "Investigation of Radiation Damage in the SLD CCD Vertex Detector," 2003 IEEE Nuclear Science Symposium, Portland, October, 2003, [http://www.slac.stanford.edu/~sinev/talks/sinev\\_IEEE2003.ppt](http://www.slac.stanford.edu/~sinev/talks/sinev_IEEE2003.ppt);  
N. Sinev, "Radiation Hardness of CCDs," LCD Meeting, SLAC, August 20, 2002, <http://www-sldnt.slac.stanford.edu/nld/meetings/2002/20020820/RadHard.pdf>.

### 3.1 Neutron Damage Studies

Our neutron damage studies of several years ago<sup>6</sup> play a key role in our current analysis of damage to VXD3 (below) but are not reported here. However, detailed study of the effects in the CCD, exposed to neutron irradiation 5 years ago, revealed new facts about the nature of radiation damage. First, we discovered that in the 5 years the CCDs sat at room temperature, no significant annealing of the damage was observed. The decrease in the number of charge traps which had been created by neutron irradiation was less than 5%. Second, we measured the dependence of the degree of charge trapping as a function of time. The trapping time expected, based on prior theory, was in the range of nanoseconds. However, we observed tens of milliseconds are required for complete trapping. We think there is a theoretical explanation, but this was overlooked in the prior theory. The effect has implication for the CCD vertex detector since it predicts less sensitivity to radiation damage effects for CCD operating at higher speed.

### 3.2 Electron Damage Studies.

During the past year, we exposed the spare VXD3 ladders to the NLCTA electron beam to measure the effects of radiation damage from electrons. We conducted two similar exposures of about  $5 \times 10^{11}$  e/cm<sup>2</sup> to two different ladders. The electron energy was 60 MeV. The charge transfer inefficiency through the entire CCD of 2000 rows caused by radiation damage from these electrons was about 30% for one ladder, and close to 90% for the other. This difference is not understood. It may result from different doses, although the experiment was designed to deliver the same dose in both exposures. While all beam parameters were very similar in both exposures, the dose monitor was only active during the second exposure. Another explanation could be different amounts of oxygen in the two detectors. We need more studies to understand this result. The important observation from these studies is that the number of charge traps per pixel created by electron irradiation is significantly different from that of the neutron created charge traps. This feature will allow to measure the relative fractions of neutron induced and electron induced radiation damage in VXD3.

### 3.3 VXD3 Radiation Damage Studies.

We have now removed the inactive vertex detector VXD3 from SLD and have begun making detailed measurements of the level and character of the radiation damage from three years of SLD data taking. In addition to normal running, at least once, early in the run, undamped beams were brought through the detector, exposing the CCDs to unusually large levels of radiation. The inner South CCDs

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<sup>6</sup> J.E. Brau and N. Sinev, "Operation of a CCD particle detector in the presence of bulk neutron damage," IEEE Trans. Nucl. Sci. 47, 1898 (2000).  
(<http://blueox.uoregon.edu/~jimbrau/talks/IEEE-99/ieee99.ps>)

were particularly affected as they face the beampipe. Detailed measurements are still in progress, but some preliminary conclusions can already be made. The distribution of number of charge traps/pixel indicates that damages were caused by light particles - electrons or photons. The level of damage corresponds to exposure to about  $10^{11}$  -  $10^{12}$  e/cm<sup>2</sup> (10 - 100 kRad) if the energy of electrons was similar to NLCTA electrons (60 MeV). If the electron was of higher energy, the estimate of the level of exposure level would be reduced.

### 3.4 CCD Ladder Studies

In order to minimize the support structure in the sensitive region of the vertex detector, we are investigating the “stretching” of silicon ladders to reduce the deflection due to gravity. We have found that the ladder deflection is directly related to the material factor of safety regardless of ladder thickness, assuming a fixed ladder length and width.

Our analysis was based on the following assumptions: (1) silicon is isotropic and homogeneous; (2) ladder dimensions are 25 cm by 2.2 cm with a thickness range of 50 to 100 microns; (3) uniformly-loaded simply-supported beam with an axial tensile force<sup>7</sup>. The objectives were to develop a set of plots for sag (deflection) versus axial loading for various thicknesses, to determine the relationship between material strength and sag and to determine whether a maximum sag of 10 microns (an extreme requirement) could be realized with a sufficient factor of safety.

A survey of the literature resulted in a minimum value for silicon tensile strength of 20.8 ksi<sup>8</sup>. Silicon derivatives (glass, fused quartz, etc.) typically exhibit higher strengths during short term loading. For this reason, a safety factor of around 10 is recommended for long term loading<sup>9</sup>. Therefore, our design strength was approximately 2.1 ksi.

Figure 1 illustrates a deformed ladder from our finite element analysis. Figure 2 shows the relationship between sag and axial tension for the thickness extremes of 50 and 100 microns. The sag is dramatically reduced initially and levels off at the load increases. The stress transforms from pure bending to almost pure tensile. Tensile stress is a function of tensile load divided by the cross-sectional area. Figure 2 shows the relationship between deflection and safety factor for the entire range of ladder thicknesses. Note that a factor of safety of 10 would result in a deflection of approximately 12 microns. Boundary condition effects are being studied

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<sup>7</sup> Young, Warren C. Roark's Formulas for Stress & Strain (6<sup>th</sup> Ed.). Table 11(e), p. 177.

<sup>8</sup> Steinzig, Mike. Bend Tests of Silicon Ladders to Determine Ultimate Strength. HYTEC Report HTN-102050-0016 (8/3/2000). Table 1, p. 6.

<sup>9</sup> Boyd, David C., Paul S. Danielson, David A. Thompson. “Glass” Kirk-Othmer Encyclopedia of Chemical Technology (4<sup>th</sup> Ed.). Vol. 12, pp. 583-584.

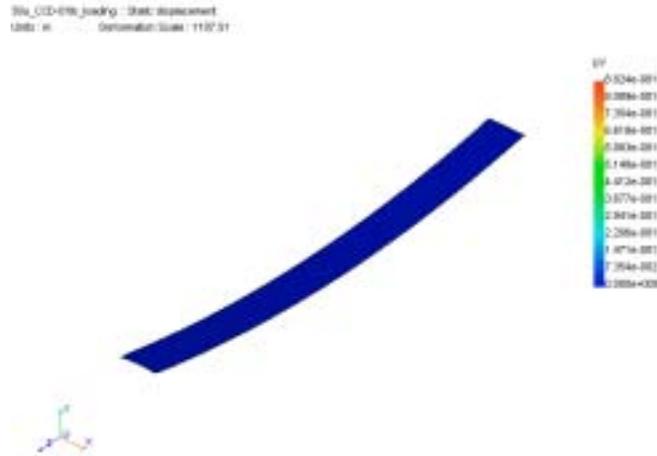


Figure 1: Deformed CCD Ladder

VXD CCD Sag vs. Axial Loading

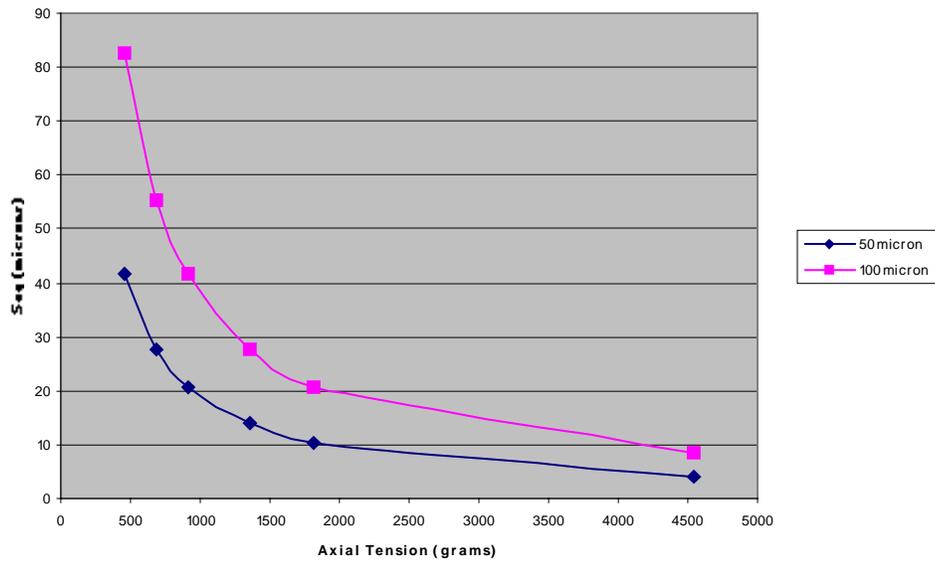


Figure 2: VXD CCD Sag vs. Axial Loading

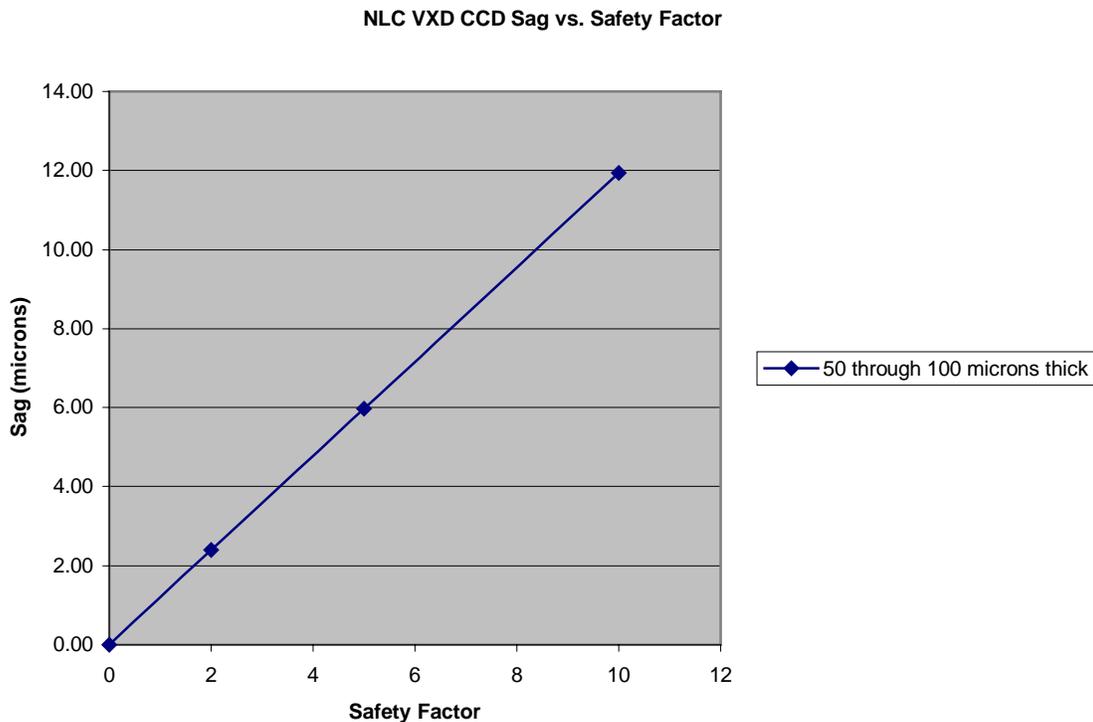


Figure 3: VXD CCD Sag vs. Safety Factor

### 3.5 CCD Design and Fabrication Studies

We have had several discussions and visits with the SARNOFF Corp. who successfully developed and built the CCD for the large format (112 CCD) Camera now in use at the Palomar Schmidt Telescope (QUEST project). SARNOFF expressed a willingness to work with us to design, prototype, and eventually build the CCD suitable for use in an NLC Vertex Detector. A rough conceptual design is emerging from these discussions. Using 6 inch wafer technology, CCD devices 22 mm x 125 mm are possible, as called for in our preliminary design for an NLC Vertex Detector. With 20  $\mu$  x 20  $\mu$  pixels this means 1100 pixels wide and 6250 pixels long CCD. The parallel clocking would be in the long directions so that all of the connecting pads would be on the outside edge, without leads or connections in the sensitive region of the detector. Each CCD would have 44 output amplifiers along the narrow outside edge, so that the serial clocking would read out 25 columns of 6250 pixels on each output amplifier. A read-out rate of 25 MHz is possible, for a total read out time of around 6 msec, which is fast enough to read out after each 190 bunches of an NLC pulse train in the 8.3 msec interval between pulse trains. With some development a 50 MHz read-out rate should be

achievable providing a large safety margin or a reduction of the number of read out amplifiers to 22 per CCD. The SARNOFF process would allow these devices to be thinned to the desired 50 to 100 micron thickness to reduce multiple scattering. Radiation hardness is an issue that would need to be addressed in the design and testing stage of this process.

### 3.6 CCD readout electronics

This year, in collaboration with SLAC, we have written a preliminary design specification document for the CCD readout ASIC.<sup>10</sup> This document defines the functionality, environment, radiation exposure, and accessibility requirements of the readout chip. The goal for this device is to provide all clocking and analog data required by an 18 readout node CCD, reduce the data by use of selectable thresholded kernels, and then transmit the data by an optical fiber to a simple event building module. It is assumed that the overall clock is external to provide flexibility, such as the possibly to deal with the eventual radiation damage, requiring slower operation.

### 3.7 CMOS Pixel Imager Studies

In our discussions with SARNOFF we discussed their well developed CMOS pixel imager process. In these devices the sensitive pixel detector and the electronics associated with each pixel are integrated on the same piece of silicon, allowing a thin detector without the need for bump bonding of two silicon layers needed in the hybrid Active Pixel devices used at the LHC. Another significant advantage of the CMOS devices is that the SARNOFF process allows pixels as small as 5 microns x 5 microns. Pixels this small would allow us to achieve the desired few micron resolution with digital (i.e., hit or no hit) output from each pixel, simplifying the read out and the electronics. The local intelligence provided at the pixel level electronics would allow an output strategy of reading out the (x,y) coordinates of only those pixels that have been hit. The read-out rate is not clear at this point, but depending on the detailed design, rates of 25 MHz seem feasible.

Assuming the above characteristics of CMOS devices, we developed the following rough conceptual designs. Devices 22 mm wide by 125 mm long called for in our preliminary vertex detector design are possible. The read-out rate required for the NLC are easy, and even a design to accommodate the more demanding TESLA read out rates seem feasible.

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<sup>10</sup> J. Brau, M. Breidenbach, and G. Haller, "LC CCD Vertex Detector Readout Electronics, Version 0.0", 2003.

- a) For the NLC, calculations indicate a background rate of 0.01 hits/mm<sup>2</sup>/bunch crossing. For a 190 bunch train this means 2 hits/mm<sup>2</sup>/train or 5500 hits/CCD for the 22 x 125 = 2750 mm<sup>2</sup> device. Reading out only the hit pixels (digitally, with x,y coordinates and a time) at 25 MHz allows a read out in ~ 0.2 millisecc, well within the available 8.3 millisecc interval between trains.
- b) For TESLA, the estimated background rate is 0.03 hits/mm<sup>2</sup>/bunch crossing. Integrating this background over the 2820 bunches in a TESLA bunch train will produce an unacceptably high occupancy. In our preliminary CMOS design we propose to read out each device in the 337 nsec between individual bunches. The 125 mm long device would be divided into 25 segments of 22 mm x 5 mm each, and each of these segments would have its independent read out bus. The number of hits per segment is expected to be 0.03 hits/mm<sup>2</sup> x (22 x 5) mm<sup>2</sup> or about 3 hits/bunch crossing/segment. Reading out the hit pixels at 25 MHz allows a readout well within the 337 nsec interval between bunches. There can be buffering at the local pixel level so that readout rates averaged over many bunch crossings are what's important, and a fluctuation up in the number of hits in a particular bunch crossing can be accommodated. With some development, faster read-out rates than 25 MHz might be possible allowing a larger safety margin or reduction in the number of read out channels per device. The present preliminary vertex detector design with 5 detector layers calls for 120 devices total. With 25 output channels per device, we need a total of 3000 read out channels, which seems manageable.

## 4. Relationship to Other CCD Vertex Detector R&D Programs

4.1 The LCFI Collaboration<sup>5</sup>, in Europe led by Chris Damerell of Rutherford Labs, is developing a CCD vertex detector for the TESLA Detector. We maintain a close relationship with the work of the European group and are coordinating our activities with them to complement, rather than duplicate, their R&D effort.

- a) We are planning to concentrate initially on developing CCDs for the NLC readout timing requirements. This is a necessary first step toward the more demanding requirements for TESLA, should that be the ultimate technology for the future e<sup>+</sup> e<sup>-</sup> collider.
- b) In our R&D program, have started discussions with U.S. commercial silicon fabrication houses to develop potential partners in the design and fabrication of CCDs and CMOS pixel imagers for both the R&D prototypes and the final detector components. The CCDs for the SLD vertex detector were fabricated by the EEV Company in England. This company now is e2V Technologies. The European vertex detector R&D program of Chris Damerell, et. al, is mostly concentrating on working with e2V in their CCD development. It is quite important to develop alternate sources for these devices for a variety of reasons:

- (i) Each silicon fabricator uses different proprietary technologies and procedures and has different design rules. It is not clear which fabricator will be successful in developing a satisfactory device or who will produce the best product.
- (ii) The fabrication of the final complement of devices will be quite expensive (order of millions of dollars or so). At the time of placing an order, it will be quite important to have several potential suppliers so that competitive bidding can help to keep the costs down.
- (iii) Silicon fabrication is quite a volatile business. Fabricators are often bought or sold (Fairchild became Loral became Martin Lockheed, EEV is now e2V, etc.) and often make decisions to discontinue various product lines (such as CCDs). The risk of a single supplier deciding to unexpectedly drop out of CCD fabrication seems quite unattractive.

In the course of the design and fabrication of the Yale QUEST CCDs, we have made a number of contacts and worked with several silicon fabricators. We will build on this base of experience and initiate discussions with several potential silicon fabricators about the design of the CCDs and CMOS detectors required for a linear collider vertex detector.

4.2 The GLC Vertex Detector Collaboration<sup>11</sup>, led by Y. Sugimoto and A. Miyamoto of KEK, is also working on the issues confronting a CCD vertex detector for the linear collider. We are in direct communication with this group, and coordinating our R&D effort, and plan now to write a proposal for the Japan-US Program to develop a vertex detector prototype. They work with Hamamatsu and e2V devices.

4.3 We have begun work on the readout electronics for linear collider CCD vertex detectors in collaboration with SLAC (M. Breidenbach and G. Haller)<sup>10</sup>. There are other groups proposing to work on the fast readout electronics required for these detectors, and we plan to coordinate our efforts closely with these groups so that together we develop a coherent detector with CCDs and the electronics appropriate to read them out.

## 5. Work Plan and Deliverables

We are proposing here a three-year R&D program to address the issues discussed above. We foresee the following activities:

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<sup>11</sup> GLC Vertex Detector Collaboration, <http://acfahep.kek.jp/subg/vtx/>

### 5.1 Work Plan Year 1

- Simulation studies of the effects of detector thickness on the physics, and coordination with other groups doing simulations
- Continue the study of effects of radiation damage
- Mechanical Engineering study of support scheme
- Continue discussions with CCD designers and silicon fabrication houses
- Start detailed design of CCD for NLC/GLC
- Initiate study of CMOS detectors for LC
- Complete conceptual design of CCD readout for NLC/GLC

### 5.2 Work Plan for Year 2

- Continue the study of effects of radiation damage
- Complete detailed design for CCDs or CMOS detectors
- Buy masks for fabrication
- Place order and start fabrication of prototypes
- Continue support structure engineering design
- Begin ASIC development for readout  
(progress on year 2 work-plan will be contingent upon successful supplemental funding to pay for all engineering and masks)

### 5.3 Work Plan for Year 3

- Complete prototype detector fabrication
- Complete prototype ASIC fabrication
- Test performance of prototype detectors
- Radiation test of prototype detectors
- Complete preliminary support structure design  
(progress on year 3 work-plan will be contingent upon successful supplemental funding in years 2 and 3 to pay for all engineering and fabrication)

### 5.4 Deliverables after the 3 Year R&D Program

- Preliminary support structure design
- First prototype devices (contingent on supplemental funding)
- Performance and radiation tests of prototype devices

## 6. Budget Requests

Item	Request in Units of \$1000		
	Year 1	Year 2	Year 3
Engineering, Technician, Shop Support and Supplies			
At Oregon	25	25	25
At Yale	25	25	25
Subcontracts			
CCD/CMOS Design	25	25	0
Masks	0	25	0
CCD/CMOS Fabrication	<u>0</u>	<u>50</u>	<u>100</u>
Yearly Totals	75	150	150

## 4.2. Development and design of an LC ASIC for CCD readout and data reduction (UCLC)

### Vertex Detector

Contact person: Patrick Skubic  
email: pls@mail.nhn.ou.edu  
phone: (405) 325-3961

Boston University  
Oklahoma

Year 1: \$51,367  
Year 2: \$96,850  
Year 3: \$96,578

## 3 Vertexing

### 3.1 Development and design of an LC ASIC for CCD readout and data reduction

#### Personnel and Institution(s) requesting funding

Boston University, Physics Department: Ulrich Heintz (assoc. professor)

University of Oklahoma at Norman, Department of Physics: Patrick Skubic (professor), George Boyd (engineer)

#### Collaborators

William Wester, Fermilab

John Jaros, SLAC

Jim Brau, U. of Oregon

#### Project Leader

Patrick Skubic

pskubic@ou.edu

(405) 325-3961

#### Changes Since Preliminary Project Description

During the first year, in addition to developing ASIC specifications, we will establish a detailed hardware development plan and an engineering management plan that specifies the roles of Oklahoma, Boston U., SLAC, and Fermilab. The responsibilities and contributions of engineers at the three institutions such as G. Boyd (OU) will be defined. Hardware development will be deferred until a clear plan for the project has been developed. Work will focus on designs suitable for the forward tracking region. An irradiated CCD detector of the SLD design has been successfully read out at OU.

#### Project Overview

A high-resolution vertex detector is a crucial component of the detector for a future linear collider. An impact parameter resolution  $\sigma \approx 5\mu\text{m} \oplus 10\mu\text{m} \text{ GeV}/p \sin^{3/2} \theta$  is desired both in  $r - \phi$  and  $z$  for flavour tagging that identifies tracks coming from primary, secondary or tertiary vertices created by the decay of particles in an event [1]. Charge coupled devices (CCD) are the most established technology for large-scale pixel vertex detectors. The SLD experiment has successfully operated a 307 Mpixel CCD vertex detector [2]. The major challenges for a CCD based vertex detector at a future linear collider are in three areas:

- reducing the amount of material by thinning the substrate;
- improving radiation hardness;
- increasing the readout speed.

This proposal will address the third challenge - readout speed. We propose to develop a readout system that will demonstrate the feasibility of use of CCD's at the LC, and could lead to designs for specific experiments. Other technologies that potentially have resolutions competitive with CCD's may also be investigated. We will collaborate with groups in the US and Europe that are developing CCD detectors for the LC. We will read out the CCD's being studied by the Oregon/Yale group, and those

under development for TESLA by the Linear Collider Flavor Identification (LCFI) Collaboration in Europe. Discussions with both groups has been started.

For the vertex detector of the SLD experiment, VXD3, there were 307 million CCD pixels [2]. The electronic circuitry that was used to handle this large number of pixels was complicated, involving at least 8 to 10 FPGA chips that were on FASTBUS modules. Readout of the SLD vertex detector took about 200 ms. For a linear collider application this time must be reduced by three orders of magnitude. This challenging goal will require a long-term R&D effort. To be able to read out the LC vertex detector it will be necessary to suppress pedestals on detector and replace some (or all) of the FASTBUS module functionality with much smaller and faster circuits, possibly contained in a single chip. A parallel readout architecture will have to be implemented.

We propose an R&D program that starts with the detailed study of the present VXD3 design developed at SLAC, and other pixel detectors to understand them thoroughly and will work in collaboration with SLAC and Fermilab to develop ASIC's with improved performance. The proposed work would lead to the design of a highly efficient system, which can be used to improve the electronic performance and hence the accuracy of the detector. In order to test our chips, we propose developing a DAQ test station suitable for detector and readout bench/beam tests. During the past summer, with the help of the U. of Oregon group, an irradiated CCD detector of the SLD design was successfully read out at OU. Clock signals were provided by a pattern generator and arbitrary waveform generators. This provided a flexible way to investigate the CCD performance and we were able to obtain valuable experience with CCD detectors for the first time. The output waveforms for each row were stored on a digital oscilloscope. The proposed DAQ system will allow readout tests with our ASIC chips to be done on prototype CCD's provided by the LCFI and Oregon/Yale collaborations.

Recently, J. Jaros proposed a layout incorporating forward CCD layers consisting of disks perpendicular to the beam line. This layout has the advantage of 10% larger solid angle coverage and minimizes material traversed by forward tracks, thus improving impact parameter resolution. The work proposed here will focus on designs suitable for the forward tracking region, in contrast with the LCFI group which is focusing on central tracking (barrel) designs. This work builds on the experience we obtained while working on the ATLAS forward (disk) pixel detectors.

A complementary proposal will be submitted to the DOE LC R&D consortium by OU faculty member M. Strauss to perform simulations emphasizing the forward tracking requirements. He is well suited to this task since he developed CCD vertex detector tracking software while a member of the SLD collaboration.

This effort builds upon previous VLSI work at University of Oklahoma. Five EE Masters students completed theses on VLSI related projects as members of our group. This includes the complete design, fabrication and testing at OU of 4 generations of a mixed-mode analog multiplexer IC, the VAMUX, which was used in the CLEO III, silicon sensor QA system. Three students contributed to the development of the ATLAS pixel detector front-end readout chip, in collaboration with LBNL. We have educational licenses for Cadence and other design tools.

We have had considerable experience with Maxwell Spicelink, which is a software package which can be used extract the L, C and R parameters of metal traces and their electromagnetic interactions with surrounding materials, such as Si and dielectrics. Maxwell creates a Spice model of the circuitry from a 3-D drawing by solving the field equations using finite element analysis. This spice model can then be used in circuit simulations. These simulations would be very useful in evaluating designs of CCD's that can be read out at very high speeds, such as proposed for TESLA.

Boston University has previous experience with irradiation tests, design, and construction of the silicon strip detector for DØ and high-speed digital electronics for the level 2 silicon track trigger for

DØ. We will draw on the Electronics Design Facility at Boston University [3] as a resource, which has extensive experience in FPGA design (DØ, CMS) and ASIC design (ATLAS). The facility also provides access to the advanced design tools required, such as Mentor and Cadence.

#### **FY2004 Project Activities and Deliverables**

Presently, the VXD3 layout consists of three barrels with a total of 96 CCDs on 48 ladders with 4 outputs per CCD yielding a total of 384 outputs. These analogue outputs are digitized and applied with a clocking signal and a bias supply at the front-end (F/E) electronics whereas the FASTBUS modules are used for managing data acquisition and providing timing and control functions. The FASTBUS data acquisition modules are placed at a distance of 50 m from the F/E boards and are connected by optical fibers. For the SLD vertex detector, disruptions in the data link occurred during accelerator operation. For reduction in the amount of devices used and to make the circuit smaller for subsequent improvement in the data processing speed and reliability, we would like to develop a new design. Replacing FASTBUS module functionality with smaller chips will enable us to place them on the barrel itself, close to the F/E hybrids. This will also make it inaccessible after detector installation, so it has to be completely reliable and able to withstand the radiation environment.

The objective for the first year will be to develop a set of specifications for the ASIC such as modularity, number of gates required for the entire operation and the identification of the design methods and development tools that are appropriate for this project. We will establish a detailed hardware development plan and an engineering management plan that specifies the roles of Oklahoma, Boston U., SLAC, and Fermilab. The responsibilities and contributions of engineers at the four institutions such as G. Boyd (OU) will be defined. We will study the use of ASIC's and FPGA's to optimize the design for the LC. The specifications will be developed in close coordination with the Oregon/Yale and LCFI groups working on CCD detector development.

#### **FY2005 Project Activities and Deliverables**

During the second year the engineers at all four institutions will collaborate in the development of a prototype readout chip for CCDs, following the specifications that were developed in the first year.

In order to test prototype vertex detector elements and/or readout chips a simple data acquisition system is required, that can be operated with minimal infrastructure requirements. The Fermilab Computing Division ESE Group has developed a general purpose set of PCI Test Adapter Cards for the BTeV experiment [4][5] that will form the basis of the BTeV pixel detector test stands. These cards are also used to test the SVX4 readout chip for the silicon strip detectors for CDF and DØ. These cards feature large FPGAs that can be programmed to interact with the device to be tested. It seems that these boards could be very useful for linear collider vertex detector test stands as well. This would mainly be done by the Boston group.

We propose to obtain a few sets of these boards and assemble a test DAQ system, using a PC provided by Boston University. We will understand the capability of the system and learn how to program it. By the end of the second year we intend to have the system running in a sample data acquisition application. This may require the design of an additional interface card for the specific detector. This project is well suited in scope for a graduate student.

#### **FY2006 Project Activities and Deliverables**

During the third year the design of the readout chip will be finalized using the experience gained from the prototype tests during the previous year. The ultimate goal is to obtain a functional design

for a readout chip that establishes the technical feasibility and can serve as the starting point for a production design.

**Budget justification**

Boston University: We ask for support for a graduate student, who will work 50% on this project. The other 50% of effort of the student will be on DØ for thesis research. This project will provide the hardware experience that is a crucial part of graduate education in particle physics. The graduate student is charged at the rate for graduate assistantships set by the BU College of Arts and Sciences for 2003/04 (\$1875/month), increased by an estimated 5% per year thereafter. Half the yearly health insurance premium (\$488 in FY2004, 10% increase per year) for the graduate student is included in budget item G6. We are also asking for support for 350 hours of electrical engineering labor in years 2 and 3 at the current subsidized EDF rate of \$40/hour (in the other direct costs category). We request travel support for about three trips each in years 1 and 2, and five trips in year 3 to Fermilab or other collaborating institutions for meetings. Indirect costs are calculated at BU's rate of 61.5%. The materials budget includes one set of PCI Test Adapter boards (\$2000/set) and funds for an interface card (\$2500) in the second year and \$2500 in the second and third years for fabrication of readout chip prototypes.

University of Oklahoma: We request a modest amount of support to fund an Electrical Engineering Graduate Research Assistant. (A small tuition remission fee is listed under other direct costs.) An EE graduate student, P. Kshirsagar, has been involved in development of this proposal and would like to use this project as the basis for her thesis. Our electronics engineer, G. Boyd, who is supported by our operating grant, will also participate in the design, fabrication and testing for this project. Fermilab will contribute to the design effort. We are requesting equipment funds for chip fabrication through MOSIS and readout electronics to support development. We request travel funds to allow us to make six round trips per year to Fermilab for meetings with collaborating physicists and engineers from Fermilab and BU. Indirect costs (IDC) are calculated using the OU rate of 48% excluding equipment. OU charges IDC at the rate of 48% on the first \$25k of the subcontract with BU.

**Three-year budget, in then-year K\$: Boston University**

Item	FY2004	FY2005	FY2006	Total
Other Professionals	0	0	0	0
Graduate Students	11.250	11.813	12.404	35.5
Undergraduate Students	0	0	0	0
Total Salaries and Wages	11.250	11.813	12.404	35.467
Fringe Benefits	0	0	0	0
Total Salaries, Wages and Fringe Benefits	11.250	11.813	12.404	35.467
Equipment	0	0	0	0
Travel	1.000	1.200	2.400	4.600
Materials and Supplies	0	7.000	2.500	9.500
Other direct costs	0.488	14.536	14.590	29.614
Total direct costs	12.738	34.549	31.894	79.181
Indirect costs	7.834	21.248	19.615	48.697
Total direct and indirect costs	20.572	55.797	51.509	127.878

**Three-year budget, in then-year K\$: University of Oklahoma**

Item	FY2004	FY2005	FY2006	Total
Other Professionals	0	0	0	0
Graduate Students	12.000	13.000	14.000	39.000
Undergraduate Students	0	0	0	0
Total Salaries and Wages	12.000	13.000	14.000	39.000
Fringe Benefits	0.828	0.897	0.966	2.691
Total Salaries, Wages and Fringe Benefits	12.828	13.897	14.966	41.691
Equipment	0	10.000	15.000	25.000
Travel	0.740	5.034	4.688	10.462
Materials and Supplies	0	0	0	0
Other direct costs	0.840	0.910	0.981	2.731
Subcontract (BU)	20.572	55.797	51.509	127.878
Total direct costs	34.980	85.638	87.144	207.762
Indirect costs	6.512	9.087	9.433	25.032
Subcontract indirect cost	9.875	2.125	0	12.000
Total indirect costs	16.387	11.212	9.434	37.033
Total direct and indirect costs	51.367	96.850	96.578	244.795

**References**

- [1] J.Brau et al., "Linear Collider R&D", <http://blueox.uoregon.edu/~jimbrau/LC/LCrandd.ps>.
- [2] K. Abe, et al., "Design and Performance of the SLD vertex detector: a 307 Mpixel tracking system", Nucl. Instru. and Meth. A400 (1997) 287-343.
- [3] see web page at <http://ohm.bu.edu/edf.html>.
- [4] K. Treptow, G. Deurling, "PCI Test Adapter Card", [http://www-ese.fnal.gov/eseproj/BTeV/TestStands/PCI\\_Test\\_Adapter.doc](http://www-ese.fnal.gov/eseproj/BTeV/TestStands/PCI_Test_Adapter.doc).
- [5] J. Andresen et al., "Programmable Mezzanine Card (PMC)", [http://www-ese.fnal.gov/eseproj/BTeV/TestStands/PMC/Prgm\\_MezzanineCard.pdf](http://www-ese.fnal.gov/eseproj/BTeV/TestStands/PMC/Prgm_MezzanineCard.pdf).

## 4.3. Study of the Mechanical Behavior of Thin silicon and the Development of hybrid silicon pixels for the LC (UCLC)

### Vertex Detector

Contact person: Daniella Bortoletto  
email: [daniela@physics.purdue.edu](mailto:daniela@physics.purdue.edu)  
phone: (765) 494-5197

### Purdue

Year 1: \$46,349  
Year 2: \$72,290  
Year 3: \$78,612

### 3.2 Study of the Mechanical Behavior of Thin silicon and the Development of hybrid silicon pixels for the LC

#### Personnel and Institution(s) requesting funding

Purdue University: Daniela Bortoletto (Professor), Ian Shipsey (Professor), Kirk Arndt (Mechanical Engineer)

#### Collaborators

FERMILAB: Simon Kwan, Jim Fast, Cristian Gingu , William Wester

#### Project Leader

Daniela Bortoletto  
daniela@physics.purdue.edu  
(765) 494 5197

#### Project Overview

One of the main objectives of the linear collider is the measurement of the Higgs couplings. This requires excellent parton flavor identification. Moreover the LC physics relies on the studies with spin-polarized beam which will generate events in the forward-backward region where tracks traverse more material. Therefore it is important that the LC tracking and vertexing systems achieve excellent momentum resolution even in the forward region and for low momentum tracks, good pattern recognition, and extremely precise impact parameter resolution to distinguish secondary and tertiary vertices for flavor tagging. R&D is necessary to substantially improve the vertexing and tracking sub-detector performance that was achieved for LEP/SLC to cope with increased jet multiplicity, higher track density in more collimated jets and larger backgrounds[1].

Material minimization is important both to achieve excellent impact parameter resolution and for the precise measurement of low momentum tracks. Therefore it impacts both silicon pixels that provide precise space points near the interaction region and a silicon microstrip tracker further from the primary interaction region, and the measurement of tracks at small angle in the forward region. Hybrid pixels are one of the options under consideration in the Tesla TDR[1] for the vertex detector and the first three planes of the forward tracker. The hybrid pixel systems under construction for the LHC experiments have a material budget of  $\approx 1.7\%$  /layer. The material budget can be reduced to  $\approx 0.2\%$  /layer for LC application by connecting  $100\ \mu\text{m}$  ( $\approx 0.1\% X_0$ ) thin sensors to readout chip electronics back thinned to  $50\ \mu\text{m}$ . The material budget is then comparable to a CCD system when the cryostat is taken into account. In the case of a silicon microstrip tracker for the LC, the momentum resolution of 1 GeV/c tracks achieved by a 5 layer silicon device improves  $\delta p_T/p_T$  from  $\approx 0.2\%$  to  $0.07\%$  if the three inner layers use  $200\ \mu\text{m}$  thin silicon strip sensors instead than standard  $300\ \mu\text{m}$  thick sensors.

The goal of this proposal is the investigation of the best methods to produce and mechanically support thin silicon sensors for Linear Collider(LC) tracking and vertexing applications. The most important issue is the quality of the detector performance versus time and cost required for production. Issues of quality and cost can only be addressed in close collaboration with industrial partners. Purdue has already started a collaboration with Micron Semiconductor to explore thin silicon applications for future upgrades of the LHC (SLHC) since thin silicon requires smaller depletion voltage and therefore it is more radiation hard than standard  $\approx 300\ \mu\text{m}$  thick silicon. This development has been funded by

the DOE ADR program. We will use the same masks and the same processing to produce sufficient silicon sensors to allow for bump bonding studies at no cost to this proposal. The masks, which have been already submitted to Micron, contain both silicon microstrip and pixel sensors matching CDF run 2b microstrip sensors and the CMS pixel layout respectively. The sensors are designed to be readout with electronics already developed for the LHC and run 2b of the Tevatron. Although, the design of the sensors is not optimized for LC operation, quality, cost, and bump bonding yield are approximately independent of the readout chip and the sensor design. By using a common sensor design we will perform a cost effective investigation of the feasibility of thin silicon technology for LC. However there are insufficient funds available in the ADR alone to develop bump bonding of thin silicon which is essential for hybrid pixel development and we request these funds in this proposal. Since the development of bump bonding of thin silicon is a considerable fraction of the funds requested we concentrate our discussion on the hybrid pixel system. We estimate that a 4-5 year development program in close association with a company is needed to demonstrate thin high yield affordable bump bonded pixel detectors.

Although most attention world wide is focused on the processing and bump bonding aspects of thin silicon development, the mechanical aspect are frequently overlooked and equally challenging and will require a similar amount of time to develop. We will produce thin silicon sensors which will be bump bonded to existing electronics. These structures will be used to study the mechanical mounting and the stability of thin silicon. The mechanical studies will have an impact not only for hybrid pixels but also for CCDs, silicon microstrip detectors and other attractive thin substrate technologies such as MAPS (Monolithic Active Pixels Sensors). Clearly thin sensors and thin ROCs are crucial to develop a hybrid silicon system for the LC. In parallel and in conjunction with other groups in the US, Asia and Europe we will study with Monte Carlo the physics reach of a thin hybrid pixel system at a linear collider and optimize its design. Finally at an appropriate future time we expect to be actively engaged in comparing the sensor technologies proposed here with competing technologies.

### Physics Motivation

Physics studies have shown that jet flavor identification with high efficiency and purity is a critical element in the full exploitation of the physics potential of the Linear Collider (LC). Jet flavor identification can be achieved in the highly collimated jets expected at the LC with precise vertex detection based on pixel detector technology achieving an impact parameter resolution of

$$\sigma_{r\phi,z}(IP) = 5\mu m \oplus \frac{10\mu m GeV/c}{p \sin^{3/2} \theta}$$

or better. In this expression the first term depends on the detector intrinsic single point resolution and geometry while the second term accounts for multiple scattering.

Charged Coupled Devices (CCD) operating at the SLD have demonstrated a resolution and a material budget close and even superior to the above requirement. Improvements are needed to achieve the readout speed required for operation at future machines such as TESLA where the single bunch crossing will take place every 330 ns. For CCDs another area of concern is radiation tolerance. Studies are taking place to evaluate the radiation damage of the SLD CCDs.

Several studies have taken place in Europe aimed at investigating an alternative approach to jet flavor identification based on solid-state hybrid pixel detectors. This technology, used for vertex detectors

in the CMS and Atlas experiments at the LHC, has the advantage of fast time stamping, sparse data read out, and excellent radiation tolerance. Assuming a three layer hybrid pixel system, with the first sensitive layer at 1.2 cm radius from the interaction point and the outmost layer at 10.0 cm radius, the desired impact resolution could be achieved with a single point resolution of  $\approx 7 \mu\text{m}$  and a material budget of  $0.5\% X_0$  for each layer[2]. This material budget assumes standard  $\approx 300\mu\text{m}$  sensors connected to readout chip electronics back thinned to  $\approx 50 \mu\text{m}$ .

Research and Development in the following areas are required for further improving this technology for LC application :

1. Improvement in the point resolution, which is currently limited by the pixel readout (ROC) dimensions of  $50 \mu\text{m} \times 300 \mu\text{m}$
2. Reduction in material. The standard thickness in silicon processing is about  $300\mu\text{m}$ .

Even with the current ROC cell size, a  $\approx 7 \mu\text{m}$  point resolution can be achieved by adopting an interleaved pixel read out as shown in [2]. This approach is similar to charge sharing through capacitive coupling in silicon strip using intermediate strips [3] and it has already produced interesting results. An alternative but more attractive option is to take advantage of the advances in submicron technology for fabricating the ROC which should allow the hybrid pixel to achieve a smaller cell dimension in the near future.

A reduction in material can be achieved directly by fabricating thin silicon sensors and read-out, or by thinning the substrates after processing. The Atlas and the BTeV collaborations have already performed R&D on sensors and ROC thinning techniques for hadron colliders applications. Our proposal will investigate for the first time the production and bump bonding of ultra-thin  $100 \mu\text{m}$  pixel sensors to electronics back thinned to  $50 \mu\text{m}$ . For the LC application the reduction in the material budget is necessary to limit multiple scattering and provide excellent impact parameter resolution.

### **Current Status of Research on Thin Silicon Sensors at Purdue**

Using DOE ADR funding, the Purdue group has explored the capabilities of several vendors to produce thin silicon sensors and received quotes from two vendors, SINTEF and MICRON. Both vendors were extremely interested in developing this new product line since pixels are expected to be a common feature of future high energy physics detectors. After reviewing vendor capabilities we have submitted a mask design to MICRON.

Bump bonding is beyond the scope of the ADR proposal but it is crucial for hybrid pixel systems. MICRON is willing to contribute funds for new equipment to develop bump bonding capabilities to the ROC chip. This development could be important since it would streamline pixel production and avoid sending the sensors to a separate vendor for bump bonding.

MICRON expects to be able to provide thin silicon wafers in the following thicknesses: 65, 80, 100, 150 and  $200 \mu\text{m}$  in 4 inch technology. The six inch technology will be limited to the last three options. The ultra thin wafers are especially interesting both for the SLHC and LC. For example a detector  $50 \mu\text{m}$  thick, with  $\rho = 50\Omega\text{cm}$  will deplete at 200 V. The material would undergo type inversion at a fluence of  $10^{15}$  particles/cm<sup>2</sup> which is well beyond the LC fluence.

The plan will be to first produce the sensor wafers at the aluminum stage and to work with an external bump bonding company. MICRON will then develop the under bond metallization process and then provide bump bonding to the readout chip. The step will first require metallization of the sensors with barrier metals to prevent aluminum spiking. To develop the bump bonding, MICRON will also have to purchase or rent a Karl Suss Flip-Chip machine. This development will take place next year if we receive Linear Collider funding.

### **Unique Facilities at Purdue**

Fermilab and Purdue University are collaborating in the work proposed here. The group at Purdue University has already received funding through the DOE ADR program to study thin silicon sensor production. The proposed effort builds upon our experience in design and testing of silicon microstrip and silicon pixels for CDF and CMS. We have access to CADENCE design tools and DESSIS simulation tools. The mechanical aspects of the project build upon our experience in the mechanical design, fabrication, and assembly of the silicon detector for CLEO III, and the mechanical design and prototyping of parts of the CMS forward pixel detector.

The detector facility at Purdue University contains two fully equipped clean rooms for the design, testing and assembly of detectors for High Energy Physics. These clean rooms are part of a complex dedicated to microstructure detector development and fabrication including silicon strip and pixel devices and micro pattern gas detectors. The total clean room space is 3000 sq ft in three laboratories containing a CMM, wirebonder, electrical testing equipment, probe stations, optical tables, microscopes and high precision measuring devices. The labs are fully equipped with computer facilities for control, data acquisition and analysis. The labs have both temperature and humidity control and HEPA filtering of the airflow. Included in the clean rooms is additional space of class 1000. In a separate location there is a detector irradiation facility with an X-ray source and an ultra clean gas delivery system used for the development and testing of micro pattern gas detectors.

Other technical resources are also available, such as machine and electronic shops within the physics department, a central machine shop and state of the art facilities on campus, such as SEM, TEM (Transmission Electron Microscopy) and EDS (Energy Dispersive Spectroscopy). In addition to the technical staff, an engineer and technician, there is the normal complement of graduate students and research associates working on specific projects. There is also an exceptional pool of talented undergraduates who work on R&D and detector construction projects.

### **FY2004 Project Activities and Deliverables**

About 20% of our effort during FY2004 will be dedicated to collaboration with European groups to establish the physics reach of a hybrid pixel system for the LC. This will include a focused simulation program to estimate the performance of a thin hybrid pixel system in collaboration with the LC tracking and vertexing simulation group. Simulation of the interleaved pixel layout and/or smaller cell size will also be conducted. We will also study the impact of thin silicon on the performance of the forward tracking system.

We expect to receive the first thin sensors in 2004. This will enable us to start a serious program of material characterization and evaluation first with microstrip sensors. The investigation of the material and device properties which are necessary to improve device design will require careful device characterization. Simulation will be required to gain a detailed understanding of device behavior and

develop predictive tools for improving device design. The tasks needed to complete this characterization and evaluation program are:

- Measurement of the device DC properties
- Characterization of the active volume of the device and optimization of the Charge Collection Efficiency (CCE)
- Tests of the device response and measurement of pulse shape.

The outcome of these studies will be a determination of the minimum thickness that can be achieved in single sided pixel manufacturing. We also plan to start working with Micron to develop the bump bonding of thinned electronics to thin sensors wafers.

The first year deliverable will be a systematic study of the characteristics of thin silicon microstrip sensors and first results from device and physics simulation studies.

### **FY2005 Project Activities and Deliverables**

In the second year we expect to receive the first thin silicon pixel bump bonded to thinned electronics. This will enable studies of the mechanical mounting and the stability of thin silicon hybrid pixels.

1. Studies of alignment and fabrication of low mass support frames will be conducted at Purdue. Metrology of thin silicon samples will be performed during cooling cycles. These will need to be conducted at cryogenic temperatures for CCD applications.
2. Finite Element Analysis (FEA) will be performed at Fermilab to understand the mechanical stability of thin silicon.
3. The Fermilab group will share the results of their R&D studies of thinning the ROC and silicon sensors that they are performing for BTeV. Interleaved pixel sensors, which are available on the BTeV wafers, will be used to build prototypes to gain more experience on the performance of interleaved thin pixels.

We will also continue the simulation of the hybrid pixel configuration.

The second year deliverable will be a systematic study of the stability issues associated with thin silicon hybrid pixels. Information will be gained on the performance potential of interleaved hybrid technology for the LC.

### **FY2006 Project Activities and Deliverables**

In the third year we will continue the simulation effort and the mechanical studies. Systematic studies will be performed with the bump bonded pixels to determine the resolution and charge collection efficiency of the prototype hybrid pixels with cosmic rays, laser diodes, and possibly beam tests. We will compare MC simulations conducted at Purdue to the performance of the pixels readout with the CMS chip.

The third year deliverable will be a first evaluation of the potential gain in resolution that can be achieved with thin, interleaved hybrid sensors. We expect to perform:

- Beam tests for structures wire-bonded to electronics.
- Tests of structures bump-bonded to readout electronics.

- Simulation of charge collection properties of structures, with both two-dimensional and three-dimensional simulation packages, CCE, pulse shape, operating conditions etc.

Many of these investigation will be done in conjunction with studies for the LHC.

### **Budget justification**

We request funds to support 50% of a graduate student. The remainder of the support of this student will come from the Purdue CDF group. The graduate student is charged at the rate set by Purdue University for 2003/2004, increased by an estimated 5% per year thereafter. We also request funds to support 50% of a postdoc during year 2 and 3 of our proposal. The remainder of the support of the postdoc will come from the Purdue CDF and CLEO group. The postdoc and the graduate student will carry out the simulation studies and will evaluate the thin silicon sensors.

We request travel support for about 3 trips each year to institutions working on LC vertexing. We are also asking for equipment items.

#### **First Year Budget**

During the first year we request \$ 25K to support the development of bump bonding with a vendor.

#### **Second Year Budget**

The second year equipment budget will allow Purdue to build a system to study the mechanical issues connected with the thinning of sensors and readout chips. The study will include precision measurement of the stability of the support schemes including temperature cycles. Some of these studies will be conducted with blank silicon and some with sensors built using ADR funds. The graduate student at Purdue will work closely with the Purdue mechanical engineer to perform the temperature cycling studies. Thin sensors provided by the ADR funding will allow a determination of the yield and the minimum thickness that is achievable by the vendors. Finite element analysis (FEA) studies will be carried out by Fermilab personnel supported by Fermilab funding.

Equipment breakdown:

1. **Precision alignment tooling: \$1.5K**  
Vacuum holders for sensor/ROC assemblies and holder for support frame that precisely aligns the modules to the support frames. Cost is based on recent experience with similar tooling for CMS pixel R&D efforts.
2. **Fabrication and assembly of a low-mass support frame: \$2.2K**  
Support frame will be either beryllium or carbon composite and will need to be of reasonably high precision.
3. **Thinned silicon, 2 batches @ \$1K per batch: \$2K (at no cost - ADR funding)** Cost estimate is based on previous purchases.
4. **Metrology: \$2.0K** This involves modifications to allow us to mount our samples in a dry chamber at low temperature in order to be optically inspected through a window. This will be similar to a chamber built by BTeV for their pixel studies but modified to allow for operation at cryogenic temperature.
5. **Engineering analysis (FEA): \$1.5 K (at no cost - supported by Fermilab)** This allows for 30 hours of engineering analysis by the FNAL analysis group.

#### **Third Year Budget**

The third year requires support for a cosmic ray and a laser setup with interleaved pixel prototypes matching an existing ROC chip (BTeV or CMS). It also funds the simulation activities that will start at Purdue.

**Three-year budget, in then-year K\$: Purdue University**

Item	FY2004	FY2005	FY2006	Total
Postdoctoral Associate		20.755	21.377	42.132
Graduate Students	9.526	9.812	10.107	29.445
Total Salaries and Wages	9.526	30.567	31.484	71.577
Fringe Benefits	0.451	9.019	9.317	18.787
Total Salaries, Wages and Fringe Benefits	9.997	39.586	40.801	90.384
Equipment	25.000	5.700	10.000	40.700
Travel	2.500	2.500	2.500	7.500
Materials and Supplies	0	0	0	0
Other direct costs	2.384	2.619	2.794	7.797
Total direct costs	39.861	50.405	56.095	146.361
Indirect costs	6.488	21.884	22.517	50.889
Total direct and indirect costs	46.349	72.290	78.612	197.251

## References

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