Precision vertex reconstruction at the ILC requires a detector capable of exquisite spatial resolution while withstanding significant low momentum charged particle fluxes and modest radiation damage. Lessons can be learned from the development of an ultra-thin CMOS pixel detector device for the high-occupancy environment of a Super B-Factory. The Continuous Acquisition Pixel (CAP) detector is based upon a Monolithic Active Pixel Sensor (MAPS) architecture fabricated in a commercially available CMOS process. What distinguishes the CAP is pipelining within each pixel cell that allows for great robustness against large hit rates, while maintaining excellent spatial resolution. These characteristics, in addition to options to expand the pixel-level signal processing, make it an ideal technology for a future International Linear Collider (ILC) vertex detector.

We propose to evolve the CAP architecture and verify the suitability of this MAPS technology for the ILC through a sequence of two prototype devices.

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A Continuous Acquisition Pixel [CAP]

FIG. 1: The CAP architecture allows optimization of the sampling functionality to be made based upon the collision environment. In both the Super B Factory and ILC cases, this optimization involves taking advantage of the machine bunch structure to minimize power consumption – a necessity for operating an ultra-thin silicon detector.

B. Choice of Technology

Until recently, the state-of-the-art in precision vertexing with pixels has been defined by the success of the CCD-based SLD detector [8] and the hybrid (sensor and ASIC readout electronics – bump-bonded together) devices developed for the ATLAS [9] and CMS [10, 11] detectors. However, despite the utility of these two types of pixel detectors for their particle physics experiments, they are not well matched to an ILC detector. Such LHC-type hybrid pixel detectors are too thick and have poor transverse resolution in each plane, which degrades the vertexing performance below Super-B [7, 12] and ILC requirements. While CCDs have impressive performance, as of yet their radiation hardness is insufficient [13] and their readout times are too long, or equivalently occupancy too high.

In the last few years groups in Strasbourg [14], LBNL [15], Hawaii [3] and others [16] have reported promising initial results with prototypes of so-called Monolithic Active Pixel Sensors (MAPS), which are thin, radiation-hard monolithic pixel detectors based on CMOS technology. A comparison between the standard Double-Sided Strip Detectors employed in Belle and a MAPS detector is shown in Fig. 2.

In MAPS the silicon epitaxial layer upon which the readout electronics are fabricated is used as the detection medium. This has the distinct advantage of providing a very thin detector with no need for bump-bonding or high-voltage biasing. Despite these promising initial results, no group has yet operated a MAPS-based detector in a running experiment. Indeed, before doing so, the following key issues need to be addressed:

1. Radiation Hardness
2. Readout Speed
3. Full-sized Detector
4. Thin (50µm thick) Detector Construction

To address these fundamental issues, a systematic development program has been established by the proposer.
C. The CAP Architecture

The operating principle of the Continuous Acquisition Pixel (CAP) architecture is illustrated in Fig. 3. The fundamental unit is a 22.5 μm square pixel cell with a 3-transistor readout circuit (shown at the upper left part of the figure). Ionization electrons diffuse onto the gate of transistor M2, which forms the collection electrode. Since the collected charges are small, they are not transferred directly to the readout bus, but rather the threshold shift of M2 is detected by a sense current applied via individual pixel addressing through transistor M3. Transistor M1 resets the electrode potential at the end of each readout cycle.

\[ \frac{1}{9 \mu s} \times \frac{2k \text{ pix}}{\text{mm}^2} \times 0.01 \frac{\text{hits}}{\text{pix}} \approx 2M \frac{\text{hits}}{\text{mm}^2 \cdot s} \quad (1) \]

which corresponds to a severe 16 MHz single silicon strip hit rate.

II. RESULTS OF PRIOR SUPPORT

The results shown below have largely been supported by the US-Japan Foundation, with funds coordinated through KEK and Fermi National Accelerator Laboratory. Additional salary support for participation by members of the University of Hawaii High Energy Physics Group is provided through DOE Contract DE-FG02-04ER41291.

A. CAP Version 1

In order to gain experience with the capabilities and limitations of the MAPS technology, a first-generation device, designated CAP1, was developed by the Hawaii group as shown in Fig. 4.

Fabricated in the TSMC 0.35 μm CMOS process [17], it consists of an array of 132 by 48 pixels, each 22.5 μm × 22.5 μm.

A critical feature is the use of Correlated Double Sampling (CDS) to remove the intrinsic channel dispersion, as well as noise/quantum uncertainty due to reset. This process is illustrated in Fig. 5, which shows data taken with a radioactive source and an 8 ms sampling time. First differences are formed between samples from just after and just before a beam cycle that has produced a trigger of interest. A channel-by-channel leakage current correction is then applied.
Frame 1 - Frame 2 = 8ms integration

- Leakage current
  Correction

~fA leakage current (typ)
~18fA for hottest pixel shown

Hit candidate!

FIG. 5: Graphic illustration of the Correlated Double Sampling and leakage current subtraction steps used to cleanly identify hit candidates in the CAP pixel detector.

Here when the difference is taken between successive sample frames, some peaks can be seen. Some of these are due to “hot” channels, i.e. channels that are known to have high leakage current. Of these more than 6,000 pixels shown, the worst case leakage current is only 18fA. These are removed in the second step, when the channel-by-channel leakage current subtraction is made. After this, the hit candidate is clearly visible. The 8ms integration time for the test arrangement shown in the figure is almost 1,000 times longer than we plan to use at KEKB, there the leakage current will be negligible.

Figure 6 is an example of an event where a high energy particle traverses a stack of four CAP pixel detectors.

FIG. 6: Detected event where a high energy particle traverses four CAP pixels. Note that the detectors are slightly misaligned.
CAP1 Readout and Radiation Hardness. A crucial feature of deep sub-micron CMOS is its resistance to radiation damage. This was the key to earlier work by Varner [19] with others that resulted in an improvement of the radiation hardness of the Belle silicon vertex detector readout electronics. In order to evaluate radiation hardness and readout speed, the CAP1 was mounted into a readout board as seen in Fig. 7.

This choice of form factor proved very versatile, as all power and control could be provided over a single set of standard unshielded ethernet cable. All signals in and out are completely differential, to reduce radiated emissions. Even with a long cable, single pixel noise values of 16e− were observed.

A series of radiation tests were performed with this set-up and are plotted in Fig. 8. Here the leakage current is plotted versus radiation dose for various periods of annealing, where the zero irradiation and 200kRad points are highlighted in the inset figure, demonstrating the clear evolution and spread in leakage current of all 6336 pixels as a function of irradiation. The accelerated dose rates are conservative when compared with an example from the published literature [20], made in the same fabrication process, shown as data points for comparison. These points correspond to slow exposure rates that are more like those that will occur in actual operation. (Practical limits on access to radiation sources precluded following the methodology of Ref. [20], though it will be considered for a final detector design.)

Even if we take the worst-case numbers from our measurements and extrapolate to the short (i.e. 9 µs) integration times planned for Super Belle, the impact of these leakage currents will be minimal. A larger concern is the possible reduction in the charge collection efficiency, a topic that is being actively pursued. Recent results indicate [21] no charge collection efficiency loss up to at least 1MRad of 1 MeV γ exposure, which is the relevant damage benchmark for a B-factory environment.

B. CAP Version 2 (Pipelined)

A limitation observed during the testing of CAP1 was the readout rate that was actually achievable. While the small die could be read at the necessary 100kHz (10µs) frame rate, scaling to a larger detector indicated problems. A solution to the problem is to place pipeline storage inside each pixel, to decouple the sampling rate from the triggered readout rate. Therefore, in CAP2 a small, 8-deep pipeline was placed inside each pixel, as seen in Fig. 9. Here, the TSMC 0.35µm process was used again.

On the left, the standard 3-pixel cell is augmented with an array of 8 selectable storage cells. The outputs are independently accessible, completely decoupling storage from reading operations. On the right is the actual pixel cell layout, with various mask layers of different colors, indicating complete utilization of the available pixel area.
C. Beam Test Results

In order to evaluate the performance of CAP1 and CAP2 beam tests were performed at KEK and Fermilab. The same basic setup was used in both cases and seen in Fig. 10. The two views on the right show the array of 4 pixels located on the beamline; at the top, a clear view showing the co-alignment of the detectors and the bottom indicating the small footprint and required cabling plant. In the lower left figure may be seen the compact PCI crate containing the Backend (B-board) readout controller and embedded CPU. This test assembly is compact and self-contained, which makes it easy to deploy for beam tests of opportunity.

Many results have been reported from these tests [2, 3]. These include measurements of charge spread, SNR and noise level. A spatial resolution of just under 11µm at KEK as seen in Fig. 11. At top left is the detector layout. At top right is shown a residual self-determination method that uses Layer 4 [L4] and L2 to project onto L3 and compare with the L3 independent determination. The resultant residual histograms in the two axes perpendicular to the test beam are shown at the bottom left.

These resolutions are consistent with GEANT simulations of the detector spacing and materials used, which indicates that multiple-scattering dominates over the intrinsic resolution for this detector configuration with the relatively low momentum π beam used.
D. CAP Version 3 (full-scale)

One of the lessons learned from CAP2 was that with only 4 metal routing layers, insufficient power distribution caused significant baseline stability problems. To address this and to provide additional storage within each pixel, a third generation of CAP detector, designated CAP3, was fabricated.

![Diagram of CAP3 pixel cell block diagram and layout.](image)

**FIG. 12:** CAP3 pixel cell block diagram and layout.

In Fig. 12 is seen the schematic representation (left) and layout diagram (right). Fabrication was moved to the TSMC 0.25\(\mu\)m process allowing an increase in the number of routing layers to 5, which improves power distribution and allows for 10 storage cells (8 for CAP2) within each pixel.

![Diagram of pixel detector to Belle Data Acquisition system.](image)

**FIG. 14:** Engineering 3D model of a CAP3 ladder configuration, consisting of 6 ladders, each of which have 4 CAP3 sensors axially by 8 sensors in width. Experience gained in support and heat conduction will be valuable in considering a larger ILC detector array.

Indeed, the CAP3 detector is large enough to be considered for the basic building block of a complete pixel vertex subdetector, as drawn in Fig. 14 and in the process of preliminary mechanical design.

![Diagram of planned data flow from pixel detector to Belle Data Acquisition system.](image)

**FIG. 15:** Planned data flow from pixel detector to Belle Data Acquisition system. A key element in this chain is the PIXRO1 chip, which is common to an ILC readout scheme.

b. Full readout chain. A crucial element of making a functional pixel detector subsystem is the ability to broadcast the data with low noise and power from the detector. The space allocated for this, at the interface between the detector and accelerator, is extremely congested and careful planning and monolithic integration are required to make such a system viable. A compact readout-flow scheme is illustrated in Fig. 15. CDS pairs are broadcast from the CAP3 detector and are analog-differenced and multiplexed in the nearby pixel readout chip (PIXRO1) [6] onto a single, high-speed analog fiber link to the electronics hut. Preliminary SPICE results indicate promising performance.
III. PROPOSED ACTIVITIES

We propose to design, fabricate and test two generations of evolutionary descendants of the CAP architecture tailored to the planned ILC operating environment.

A. ILC Prototype

While the operating environments in the inner detection layers at Super B and the International Linear Collider are different, the requirements on thickness, data volume, low-power consumption and the instantaneous occupancy are actually quite similar, as may be seen in Table I. In these comparisons integration time is dependent upon the reset and sampling times needed, which is in turn related to the machine bunch structure shown in Fig. 1. In both cases the electronics operation is optimized to reflect the machine structure available, as described below. For the ILC, there are two options listed for some parameters, with the first for technologies capable of storing samples within a bunch train (Column Parallel CCD (CPCCD) with storage or CAP) and the second with longer integration time (higher occupancy) corresponding to devices without in-pixel storage (standard CCD or DEPFET).

Of the comparisons listed, it is interesting to note that the data rate and radiation tolerance requirements are actually more severe for Super Belle than for the ILC [22]. That is, any detector capable of successful operation in the Super B environment is a viable option for the ILC vertex detector.

1. Optimizing CAP architecture

We plan to pursue two generations of ILC-specific CAP design, designated LCAP1(2), optimized for the ILC beam structure. As the CAP architecture is quite flexible, it can be tailored for the machine operational environments, as mentioned earlier in Fig. 1. The first generation will explore issues of maximum sample storage depth. A second generation will follow-up with lessons learned, as well as exploring ultra low-power operation, a major concern for reducing support infrastructure.

Discussions have begun [24] on possible joint collaborative efforts to make a variant of the CAP architecture that is tailored to the ILC requirements. These discussions have affirmed that a device suitable for a high-luminosity Belle could also serve as a functioning prototype for a future ILC vertex detector. Given the long and uncertain development time table for completion of the ILC detector, it makes sense to develop experience through the completion and commission of a working pixel vertex detector system under demanding operating conditions.

2. T-943 at Fermilab

Varner is spokesperson for the T-943 experiment at Fermilab, which has the charge of evaluating the ultimate resolution of high sensitivity, pipeline operation MAPS devices. Evaluation of both generations of LCAP detector will be performed at the Meson Test Beam Facility [25], where it will be necessary to have very high energy, minimum ionizing particles (120GeV/c protons) to confirm that the single-point resolution meets the $\mu$m-level ILC requirement.

B. Task Sharing

In addition to members in Hawaii, the Belle pixel group consists of physicists and engineers from the KEK laboratory, the University of Tsukuba (Japan), the H. Niewoniczanski Institute of Nuclear Physics in Krakow (Poland), the University of Pittsburgh, the Nova Gorica Polytechnic Institute (Slovenia), the University of Melbourne (Australia) and the University of Tokyo.

CAP Pixel. While Varner is the leader of this project, he is well aware that successful completion of a project of this scale requires multi-institutional resources. A breakdown of task sharing for the Belle pixel effort is provided in Table II.

These institutional responsibilities are a logical continuation of current activities within the Silicon Vertex Detector group. The Krakow group has built the readout chain for the current and original SVD, with KEK providing mechanical, integration and infrastructure support. Melbourne built most of the production silicon ladders that have been used in Belle and will be available for production work once they have concluded their ATLAS endcap silicon assembly. Radiation and environmental monitoring will be performed by Nova Gorica Polytechnical, with support from the Univ. of Tsukuba. Hawaii will focus on detector design and ladder mechanical structure. The Tokyo and Pittsburgh groups will focus on pixel vertex detector testing, evaluation and simulation.

All these groups have expressed interest in extending this effort toward an ILC vertex detector. To the list of institutions above, Ray Yarema’s group at Fermilab has also joined this development effort.
TABLE I: Comparison of Super B-Factory and ILC pixel vertex detector operating conditions. For the ILC there are often two parameters listed with a slash between, referring to the possible choice between candidate technologies. As no single technology has demonstrated itself capable of meeting all of the design and environmental requirements, it is expected that this R&D effort should remain active for the next few years, with a decision to be made in 2010 at the earliest [23]. Evolution of the CAP technology to meet these requirements shows real promise.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>ILC</th>
<th>Super-B</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integration time</td>
<td>25µs/1ms</td>
<td>≤ 10µs</td>
<td>Belle (trigger dep.)</td>
</tr>
<tr>
<td>BX collision timing</td>
<td>300 (150) ns</td>
<td>2 ns</td>
<td></td>
</tr>
<tr>
<td># bunches/integ. time</td>
<td>75(150)/2.8k</td>
<td>1-5k</td>
<td>CPCCD or MAPS/DEPFET for ILC</td>
</tr>
<tr>
<td>Expected occupancy</td>
<td>≈ 1%</td>
<td>≈ 0.5−1%</td>
<td>Belle extrapolation (max.)</td>
</tr>
<tr>
<td># pixel channels (Million)</td>
<td>100’s to 1k</td>
<td>10-50</td>
<td>5 layers versus single</td>
</tr>
<tr>
<td>Duty cycle (high power)</td>
<td>few %</td>
<td>5-10%</td>
<td>within acceptance</td>
</tr>
<tr>
<td>Readout cycle</td>
<td>between trains</td>
<td>continuous</td>
<td></td>
</tr>
<tr>
<td>Pixel readout rate (raw)</td>
<td>500/10 Gpix/s</td>
<td>200-1000 Gpix/s</td>
<td>Belle 10kHz trigger</td>
</tr>
<tr>
<td>Radiation requirements</td>
<td>0.5kGy/yr</td>
<td>few 10kGy/yr</td>
<td>neutron dose not considered</td>
</tr>
</tbody>
</table>

TABLE II: CAP Pixel Collaboration.

<table>
<thead>
<tr>
<th>Institution</th>
<th>Resource</th>
<th>Contact</th>
</tr>
</thead>
<tbody>
<tr>
<td>INP, Krakow</td>
<td>Readout Elec.</td>
<td>H. Palka</td>
</tr>
<tr>
<td>KEK</td>
<td>Infrastructure</td>
<td>T. Tsuboyama</td>
</tr>
<tr>
<td>Nova Gorica Puly</td>
<td>Rad. monitor</td>
<td>S. Stanic</td>
</tr>
<tr>
<td>Univ. Hawaii</td>
<td>Detector</td>
<td>G. Varner</td>
</tr>
<tr>
<td>Univ. Melbourne</td>
<td>Production</td>
<td>G. Taylor</td>
</tr>
<tr>
<td>Univ. Pittsburgh</td>
<td>Analysis</td>
<td>J. Mueller</td>
</tr>
<tr>
<td>Univ. Tokyo</td>
<td>Testing</td>
<td>H. Aihara</td>
</tr>
<tr>
<td>Univ. Tsukuba</td>
<td>Environ.</td>
<td>Y. Asano</td>
</tr>
</tbody>
</table>

The Fermilab group brings the resources of an excellent engineering group to collaborate on the design for an ILC-specific pixel detector. The details of task sharing are under discussion at this time and will be guided by the financial support that can be garnered.

IV. BROADER IMPACT

As one of the founding mentors, Varner was instrumental in establishing the Quarknet program in Hawaii. Being separated from the US mainland and Asia by thousands of miles of open ocean, it is essential to expose high-school teachers and local, underserved students to the excitement of frontier physics though our local research activities. Our annual Physics Open Houses are very well-attended and being able to involve and interest the community at large is crucial.

The current UH QuarkNet program had its first teacher workshop last summer, with 10 teachers participating in a mix of lecture and hands-on lab sessions. The lectures provide particle and cosmic-ray physics education for the teachers, earning UH graduate credits, which in turn allow for their own career (and payscale) advancement providing an incentive to participate. The lab sessions involved component assembly and instruction in the operation of the cosmic-ray detectors. We propose to add to this program a “work at Fermilab” component beginning next summer, including participation in hardware fabrication, operation of equipment in the beam test and summer lecture and curricular development.

The current UH QuarkNet program provides opportunities for teachers’ professional development using the Hawaii State Department of Education (HDOE) Professional Development Credits (PDERI) program. Teachers can earn PDERI credits which advance them on their pay scale by showing evidence of the success of their activities with their students. This is done via a portfolio submitted by the teachers to external evaluators in the HDOE. For teachers, QuarkNet provides resources and partnership opportunities that the teachers have no access to otherwise. In addition, the intellectual development opportunities in QuarkNet, with hands-on activities and conceptual material that can be directly transferred to curriculum (lab exercises, science fair projects, class discussion of the latest ideas in particle astrophysics, etc.).

The final portfolios that teachers prepare for these credits under QuarkNet provide tangible and quantitative evidence of the effectiveness of the program, and we intend to track the development and impact of our proposed activities through these portfolios, through periodic review and summaries.

Public support for funding of the ILC in the long-
haul depends upon educating the educators, the next generation of students, and the general public in the exciting discovery possibilities at the ILC, and the very interesting technical challenges (some being addressed in Hawaii!) to meet them. This type of hands-on hardware exposure for the young and inquisitive researchers is sorely needed as scientific collaboration sizes have increased.

V. FACILITIES, EQUIPMENT AND OTHER RESOURCES

Considerable expertise and engineering resources are available at the University of Hawaii and our activities are well supported. We have two full-time machinists available through the Department of Physics and Astronomy machine shop, as well as the support infrastructure described below.

A. Instrumentation Development Laboratory

The CAP progress demonstrated up to this point would have been impossible without the support of an entire engineering team at the University of Hawaii. With strong support from the High Energy Physics Group, the Instrumentation Development Laboratory [26] develops world-class instrumentation such as the CAP pixel.

Dedicated to the development and support of high-performance instrumentation for world-class research in High Energy and Particle Astrophysics, the ID Lab is available to the University of Hawaii research community at large.

As can be seen in Fig. 16, the lab serves as host to a diverse group, bringing together talent from throughout Asia, Europe and North America.

Electronics design support consists of workstations and software for the design of ASICs, circuit boards, and FPGA/CPLD firmware. Assembly benches and prototyping facilities, with available and well-trained student technician support, are maintained. Test instrumentation in NIM, 6U/9U VME, CAMAC, FASTBUS, compact PCI and LabView/GPIB are available. Silicon pixel and custom detector development are facilitated by a Cascade motorized probe station, Agilent parametric analyzer, K&S wire-bonder, all located inside an assembly clean room. SMT assembly/inspection stations are complemented by a BGA rework station.

The ID-Lab provides expertise in IC and board design, as well as software and firmware. Lab chief engineer Kennedy is coordinating the pixel readout system design. Engineering doctoral fellow Martin will complete the PIXRO1 and LCAP1 design as part of her dissertation work. A particularly valuable asset is mechanical engineer Rosen, who designed the current Belle beampipe and will lead the mechanical design of the pixel ladder structure.

Excellent laboratory space is provided by the University, with over 2000 square feet available to the ID Lab, as can be seen in Fig. 17.

B. Hawaii Faculty, Researchers and Students

Faculty members Browder and Trabelsi are active participants in this project. Senior researcher Parker is a wealth of information on silicon fabrication and processing. The CAP pixel project is the primary task of post-doc Barbero. Student Uchida has participated in all beam tests, with student Sahoo to join and gain hardware experience.

Our current DOE grant supports all of these group members. Pending this award, new student Rorie will join the effort and start detailed studies of detector optimization.

a. Other Facilities In addition to the full-time machinists and shop mentioned, the university also provides computing support and access to a high-performance computer farm.
VI. FY2006 PROJECT ACTIVITIES AND DELIVERABLES

In the first year the target will be to develop a first generation of ILC-specific sampling architecture. Our current studies show that down to quite small storage cell capacitances, as shown in Fig. 18, the kTC noise looks manageable. The current design exercise is to explore the maximum packing density possible, to maximize the number of storage cells, which reduces the effective occupancy for a given integration period.

The first ASIC design is designated LCAP1 (Linear Collider CAP #1) and the development timescale is matched to a fiscal year. From experience with three generations of CAP detector, this is a reasonable interval in which to perform the tasks outlined below:

1. design – 3 months
2. fabrication – 3 months
3. eval board – 2 months
4. firmware/software – 2 months
5. test/document 2 months

The deliverables are a set of fabricated die after 6 months, a functioning die on test board, available for radiation, noise, resolution and other testing within 10 months. Finally, a publication documenting results of these tests round out the year development cycle.

VII. FY2007 PROJECT ACTIVITIES AND DELIVERABLES

In the second year we expect to have feedback not just from the LCAP1 prototype, but also for subsequent generations of Super Belle CAP pixel detector. In the latter case the experience with handling very thin devices and operating at high speed and low power will be valuable in shaping the direction of the next generation of demonstrator prototype, which would be designated LCAP2.

The development cycle and deliverables are identical to those for FY2006, with the report being delivered serving as a critical milestone at which to assess whether to take this development forward toward a full-sized detector prototype or instead recommend pursuing another strategy based upon concurrent development efforts by other groups.

VIII. PROPOSED BUDGET AND JUSTIFICATION

A summary of the proposed total budget is given in Table III. The budget is broken out by fiscal year and also by salary, travel, equipment fabrication, material & supplies and miscellaneous costs (shipping, document).

<table>
<thead>
<tr>
<th>Item</th>
<th>FY06</th>
<th>FY07</th>
<th>total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Salaries &amp; fringe</td>
<td>$17.0</td>
<td>$17.0</td>
<td>$34.0</td>
</tr>
<tr>
<td>Travel</td>
<td>$4.5</td>
<td>$4.5</td>
<td>$9.0</td>
</tr>
<tr>
<td>Equipment fabrication</td>
<td>$29.8</td>
<td>$31.2</td>
<td>$61.0</td>
</tr>
<tr>
<td>Other direct costs</td>
<td>$1.2</td>
<td>$1.2</td>
<td>$2.4</td>
</tr>
<tr>
<td>Indirect costs</td>
<td>$4.7</td>
<td>$4.7</td>
<td>$9.4</td>
</tr>
<tr>
<td>TOTAL</td>
<td>$57.2</td>
<td>$58.6</td>
<td>$115.8K</td>
</tr>
</tbody>
</table>

b. Operations. We also request half-time salary support for one graduate student who will pursue the proposed research in partial fulfillment of his dissertation requirements. A student, J. Rorie, has already been identified, and has expressed interest and willingness to participate in the research if the funds are available. The student will take his PhD qualifying exam in the spring of 2006.

We also request support for two part time undergraduate research assistants to help in performing the equipment fabrication for the work described. Required engineering resources are costed as part of specific equipment tasks listed below.

c. Travel. Travel is requested for the proposer and other participants to perform the measurements of detector performance as part of the ongoing T-943 beam test experiment at Fermilab.
d. Equipment. We describe here the major fabricated equipment costs, with ASIC fabrication through MOSIS.

Costs for the first ILC detector prototype are listed in Table IV. This prototype builds heavily on the systems developed previously. Some electrical engineering design time is required for an improved portable data acquisition system and to establish the data link. Student labor costs are not included here. Budgeting is based upon completion of the task within FY2006.

<table>
<thead>
<tr>
<th>Item</th>
<th>Est. Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCAP1 ASIC fabrication</td>
<td>$12.4K</td>
</tr>
<tr>
<td>Engineering (mechanical)</td>
<td>$2.5K</td>
</tr>
<tr>
<td>Engineering (electrical)</td>
<td>$7.5K</td>
</tr>
<tr>
<td>ICs, parts &amp; materials</td>
<td>$2K</td>
</tr>
<tr>
<td>Board fabrication</td>
<td>$2.5K</td>
</tr>
<tr>
<td>misc. cabling, housing</td>
<td>$1.5K</td>
</tr>
<tr>
<td>Test structure assembly</td>
<td>$1.4K</td>
</tr>
<tr>
<td>Estimated total</td>
<td>$29.8K</td>
</tr>
</tbody>
</table>

TABLE IV: ILC CAP “LCAP1” prototype budget.

Common to both these tasks, additional non-recurring engineering costs support the design and printed-circuit board layout capacity of the Instrumentation Development Laboratory. Stuffing and testing of the boards is supported by student labor captured separately.

Costs for a second-generation ILC detector prototype are tabulated in Table V. This prototype will be an evolution based upon lessons learned with the LCAP1 prototype. It is assumed that a deeper sub-micron process will be used, consistent with evolving industry trends. Student labor costs are again not included here. Budgeting is based upon completion of this task in FY2007.

<table>
<thead>
<tr>
<th>Item</th>
<th>Est. Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCAP2 ASIC fabrication</td>
<td>$17K</td>
</tr>
<tr>
<td>Engineering (mechanical)</td>
<td>$2K</td>
</tr>
<tr>
<td>Engineering (electrical)</td>
<td>$5K</td>
</tr>
<tr>
<td>ICs, parts &amp; materials</td>
<td>$2K</td>
</tr>
<tr>
<td>Board fabrication</td>
<td>$2.5K</td>
</tr>
<tr>
<td>misc. cabling, housing</td>
<td>$1.5K</td>
</tr>
<tr>
<td>Test structure machining</td>
<td>$1.2K</td>
</tr>
<tr>
<td>Estimated total</td>
<td>$31.2K</td>
</tr>
</tbody>
</table>

TABLE V: ILC CAP “LCAP2” prototype budget.
[16] A number of groups are pursing MAPS-based detectors for the ILC. In addition to the work at Strasbourg/DAPNIA and LBNL/Berkeley, efforts are underway at Yale/Oregon, in the U.K. (LCFI Collaboration), and probably others of which the proposer is unaware as they did not make presentations at either ILC Snowmass 2005 or PIXEL2005.
[18] Extrapolating background hit estimates from silicon strips to MAPS depends strongly on the charged particle to x-ray/γ ratio. For CAPS, the pixel is about 8,000 times smaller, has an 9 times longer integration time and the active volume is about 30 times smaller than the reference silicon strip. At 20 times background, the 10% DSSD occupancy becomes $\sim 7.5 \times 10^{-3}\%$ for all neutral and $\sim 0.225\%$ for all charged tracks.
[23] Private communication with Chris Damerell, ILC research coordinator.
[24] Private communications between the proposer and institutional representatives at Snowmass ILC meeting (August 2005) and PIXEL2005 (September 2005). There is world-wide interest in developing the CAP design for ILC operation.