

## Development of thin silicon sensors for tracking

**Classification (subsystem)** Tracker.

### **Personnel and Institution(s) requesting funding**

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### **Project Overview**

One of the possible detector options for the LC is SiD which incorporates a Silicon/Tungsten calorimeter with a precise silicon tracker and vertex detector. The tracker design includes a compact silicon tracker with 5 layers in the central region and five disks per end. The tracker is required to provide excellent momentum resolution and pattern recognition in a compact volume and thereby minimizes the cost of the calorimeter. Now that the LC technology has been selected it is important to develop the SiD detector concept into a detailed detector technical design report. In order to achieve this goal there are critical questions that have to be addressed. These questions have been summarized in a document by Breidenbach, Brau, Jaros and Weerts[1]. This proposal will address the issue of material minimization and pattern recognition in the endcap outlined in [1].

### **Material Minimization**

The objectives of LC physics include the precision studies of the Higgs and new physics which can only be achieved by a detector with:

- excellent flavor tagging efficiency and purity for bottom and charm quarks
- superb momentum resolution with polar angle coverage down to about 110 mrad.
- two jet mass resolution comparable to the natural width of the W and Z bosons
- hermeticity to achieve a precision measurement of the missing momentum

These requirements lead to a fully integrated detector and the implementation of particle flow algorithms to measure the jet energies.

Therefore it is important that the LC tracking and vertexing systems achieve excellent momentum resolution even in the forward region and for low momentum tracks, good pattern recognition, and extremely precise impact parameter resolution to distinguish secondary and tertiary vertices for flavor tagging. R&D is necessary to substantially improve the vertexing and tracking subdetector performance that was achieved for LEP/SLC to cope with increased jet multiplicity, higher track density in more collimated jets and larger backgrounds[2].

Material minimization is important both to achieve excellent impact parameter resolution and for the precise measurement of low momentum tracks. Therefore it impacts both silicon

pixels that provide precise space points near the interaction region and a silicon microstrip tracker further from the primary interaction region, and the measurement of tracks at small angle in the forward region.

Preliminary simulations have been performed comparing the momentum resolution achieved by the silicon tracker in a SD Thin and SD Thick scenario in the barrel. The results indicate that the SD thin tracker with 3 inner layers of sensors 200  $\mu\text{m}$  thick and 2 outer layer of standard thickness silicon (300  $\mu\text{m}$ ) could achieve similar or better momentum resolution than a TPC tracker[3].

Several questions must be answered in order to understand if this option is truly feasible:

- Can thin detectors be manufactured with a reasonable yield?
- What signal to noise ratio and resolution can be obtained with thin sensors?
- Can mechanical handling and mechanical support challenges be met?

The R&D program at Purdue University will answer these questions in a very cost effective and timely way.

### **Current Status of Research on Thin Silicon Sensors at Purdue**

Using DOE ADR funding, the Purdue group selected MICRON in 2003 to produce thin silicon sensors. MICRON delivered in 2004 thin silicon strip sensors in the following thicknesses: 150, 200, and 300  $\mu\text{m}$  in 4 inch technology. The sensors were manufactured using the masks developed for the silicon layer mounted on the CDF beam pipe. Each sensor is 7.84 cm long, 0.843 cm wide, with 256 channels designed to be connected to 128 readout channels. We also received double sided silicon pixel sensors on 6 inch wafers in 2004. These wafers are 200 and 300  $\mu\text{m}$  micron thick. Each  $n^+$  pixel has a dimension of 100  $\mu\text{m} \times 150 \mu\text{m}$  matching the PSI46 0.25  $\mu\text{m}$  readout chip developed for the CMS pixel detector at the LHC.

Last year we received modest funding from the Linear Collider R&D. The funding was used to partially support a graduate student to characterized the thin silicon sensors and to set-up a system to measure the response of thin silicon strip detector with an infrared laser.

#### *Sensor Characterization*

The DC characterization was performed on 150, 200 and 300  $\mu\text{m}$  thick sensors and it included measurements of the capacitance to ground and the leakage current as a function of the bias voltage. Strip-by-strip scans were also performed to measure the leakage current ( $I_{leak}$ ), the interstrip capacitance ( $C_{IS}$ ), the coupling capacitance ( $C_C$ ), the interstrip resistance ( $R_{IS}$ ) and bias resistance ( $R_{bias}$ ) at a bias voltage above the depletion voltage. The electrical performance of the thin silicon strips is summarized in Table 2. The depletion voltage of the sensors was found to scale with the thickness as expected. The 300  $\mu\text{m}$  thick sensors have a depletion voltage of about 85 V. The depletion voltage decreases to 30 and 15 V for 200  $\mu\text{m}$  and 150  $\mu\text{m}$  sensors respectively. The leakage current is usually dominated by the bulk current and it is expected to increase with the sensor thickness. In fig. 1 we compare the leakage current for 150 $\mu\text{m}$  and 300  $\mu\text{m}$  thick sensors. The current of the 150  $\mu\text{m}$  at  $V_{bias} = 2V_{depletion}$  passes the required specifications. At larger  $V_{bias}$  the current is larger and similar to that measured in 300  $\mu\text{m}$  devices indicating that the leakage current is presumably dominated by other effects such as surface current. Strip-by-strip scans verified that sensors were passing the specification of  $C_C > 10 \text{ pF/cm}$  and  $C_{IS} < 1.2 \text{ pF/cm}$ . The bias resistance

of the 200 and 150  $\mu\text{m}$  thick sensors was within the specification of  $R_{bias} = 1.5 \pm 0.5 \text{ M}\Omega$ . It was below specs for the 300  $\mu\text{m}$  thick sensors.

All seven 150  $\mu\text{m}$  thick sensors pass the specification we had set including having a leakage current below  $< 50 \text{ nA/cm}^2$  at a bias voltage equal to twice the depletion voltage. These results confirms that thin detector processing can be successfully achieved. The measurements of the capacitance and resistance indicates that the resolution performance should not be compromised by reducing the sensor's thickness.

Table 1: Comparison of DC characteristics of 300, 200 and 150  $\mu\text{m}$  thick sensors measured at Purdue University. We follow the same notation used in the text with leakage current ( $I_{leak}$ ), interstrip capacitance ( $C_{IS}$ ), coupling capacitance ( $C_C$ ), interstrip resistance ( $R_{IS}$ ) and bias resistance ( $R_{bias}$ ). We assign a grade to the sensors according to  $I_{leak}$ . Grade A (B) sensors have a  $I_{Leak}$  at  $2 \times V_{dep} < 50 \text{ nA/cm}^2$  ( $4000 \text{ nA/cm}^2$ )

	$I_{leak}$	$C_C$ pF/cm	$C_{IS}$ pF/cm	$R_{IS}$ G $\Omega$	$R_{bias}$ M $\Omega$
Specs	#, Grade A #, Grade B	$> 10$	$< 1.2$	$> 1$	$1.5 \pm 0.5$ $< 10 \%$ variation
300 $\mu\text{m}$	3, Grade A 2, Grade B	$12 \pm 0.9$	$0.9 \pm 0.03$	$> 1$	$0.5 \pm 0.2$
200 $\mu\text{m}$	3, Grade A 2, Grade B	$17 \pm 1.7$	$0.5 \pm 0.02$	$> 10$	$1.8 \pm 0.10$
150 $\mu\text{m}$	7, Grade A 0, Grade B	$16 \pm 1.3$	$0.62 \pm 0.03$	$> 10$	$1.8 \pm 0.10$

### *S/N measurements*

A critical step to fully evaluate the feasibility of thin sensors for the LC is to determine the Signal to Noise ratio (S/N) and the charge collection efficiency. In a silicon detector, the signal for a charged particle depends on the path length the particle traverses in the silicon and so S is inversely proportional to the thickness. With currently available electronics the noise is expected to be low enough that reducing the silicon thickness from 300  $\mu\text{m}$  to 200  $\mu\text{m}$  would still allow a S/N above 15. For example, the SVX4 chip has a noise of 900 electrons for a capacitive load of 20 pF while the most probable signal for a 200  $\mu\text{m}$  sensor is 14,440 electrons, yielding a S/N of 16. However, in a thin silicon sensors there is also an increased capacitive coupling between the two sides of the sensor, which might increase the noise. Maintaining an acceptable S/N is critical for the long ladder design proposed for SiD[3].

The experimental setup for the S/N measurements uses a laser illuminating a microstrip sensor wire-bonded to the SVX4 readout chip connected to a PTA/PMC based DAQ system[4] developed for Run IIb of the Tevatron. A custom made printed circuit board hosts a SVX4 ASIC and a sensor. The 1064 nm laser used in the setup has an absorption length in silicon of about 1 mm. Only 51 channels out of 128 channels of each sensor are connected to the readout chip. Fig 2 shows the custom made circuit board with the SVX4 chip wire-bonded to a thin sensor and the the laser measurement system.

After setting the laser to focus at the sensor surface, a laser scan was taken as a function of the strip position. Fig. 3 shows an example of the laser scan between strips. The laser moves from channel 50 to channel 53 of a 300  $\mu\text{m}$  thick sensor in steps of 5  $\mu\text{m}$ . Since the  $p^+$  implant

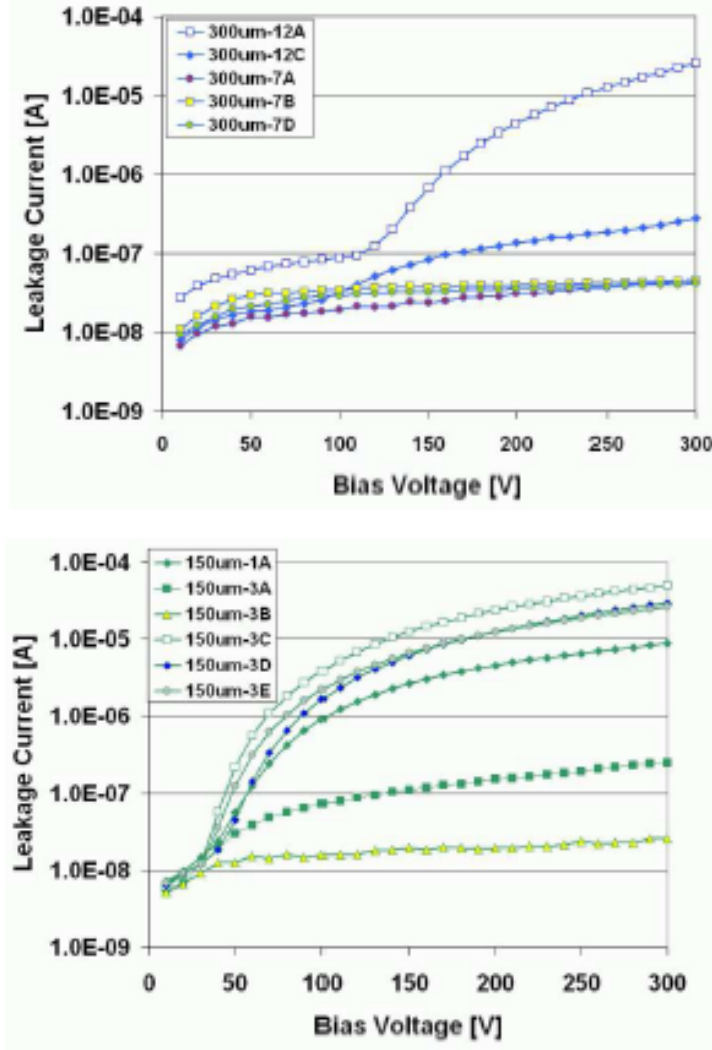


Figure 1: IV measurement for 300 and 150  $\mu\text{m}$  thick sensors.

strip is covered by metal layer of 8  $\mu\text{m}$ , most of the laser light is reflected as shown by the three valleys, one for each  $\text{p}^+$  implant, in the charge collection measurements presented in Fig. 3. Once the laser is located between two strips, most of the deposited charge is collected.

To study the S/N ratio we locate the laser between two strips to maximize the charge collection. The noise in each channel is estimated from the Gaussian dispersion ( $\sigma$ ) of the pedestal for that channel. In the current set-up, the common mode is the dominant component to the noise since the grounding of the sensor hybrid was not implemented. When proper shielding will be installed, we expect the common mode noise to be significantly reduced. The differential noise is determined by subtracting the common mode noise. The total signal was defined as the sum of the charge in the hit strips after a pedestal is subtracted. The bias voltage was set to 100 V which is above depletion voltage for all sensors. In table 2 the signal and the noise in ADC counts for various sensors are presented. The error on the signal is typically less than 1 % and the error on the noise is typically less than 3%. The signal-to-noise (S/N) ratio are about 10.5, 8 and 5.4 for 300, 200 and 150  $\mu\text{m}$  sensors respectively. The noise for all

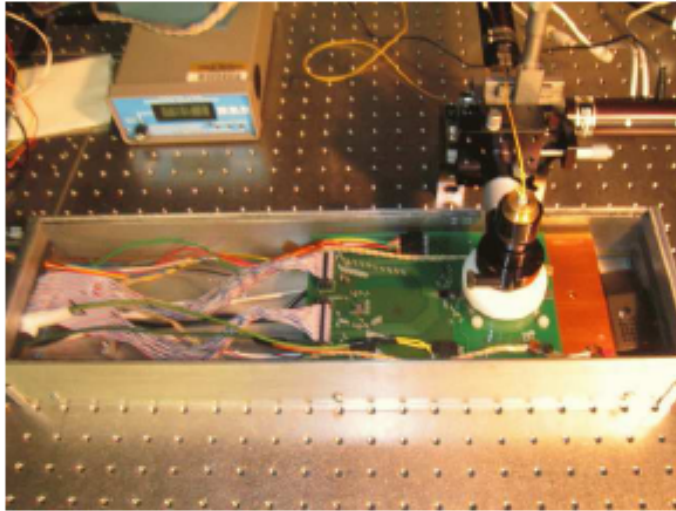


Figure 2: The laser measurement system with the sensors mounted on the adaptor board and connected to the readout chip.

sensors is about 2 ADC counts and it is independent on the thickness in agreement with the DC characterization. The S/N is about a factor of 2 smaller for 150  $\mu\text{m}$  than 300  $\mu\text{m}$  sensors. This is consistent with expectations and demonstrate the utility of thin silicon. Nonetheless, the S/N performance is disappointing even for 300  $\mu\text{m}$  thick sensor. Study of the SVX4 ROC indicate that noise of this chip is  $N=400+45 \times C$ , where C is the capacitance of a strip to ground. For our sensors the total capacitance is about 4 pF and therefore the expected noise is about 570 electrons. Assuming a most probable charge of 72e-h pairs/ $\mu\text{m}$  we expect a S/N of about 38, 25 and 19 for 300, 200 and 150  $\mu\text{m}$  thick sensors. We are investigating the discrepancy between the expectations and the results of the S/N measurements. In summary, the results from the DC characterization already at hand are extremely promising but further studies need to be performed to understand the poor S/N observed.

Table 2: The signal, noise and S/N measured with the laser system.

Sensor ID	Signal (ADC)	Noise (ADC)	S/N
300 $\mu\text{m}$	22	2.1	10.5
200 $\mu\text{m}$	15.2	1.9	8
150 $\mu\text{m}$	10.2	1.9	5.4

### Future R&D for thin silicon sensors

We will use the laser test stand already in place at Purdue to continue studies of the S/N of thin silicon sensors with the SVX4 chip. We will also irradiate the sensors with the Co60 source available at Purdue University to understand possible degradation in the detector performance due to gamma rays. Ultimate functionality and performance characteristics will be established in a test beam. We plan to take advantage of the MT4 test beam facility at Fermilab and to measure the charge collection efficiency, position resolution, and signal to noise ratio in the beam.

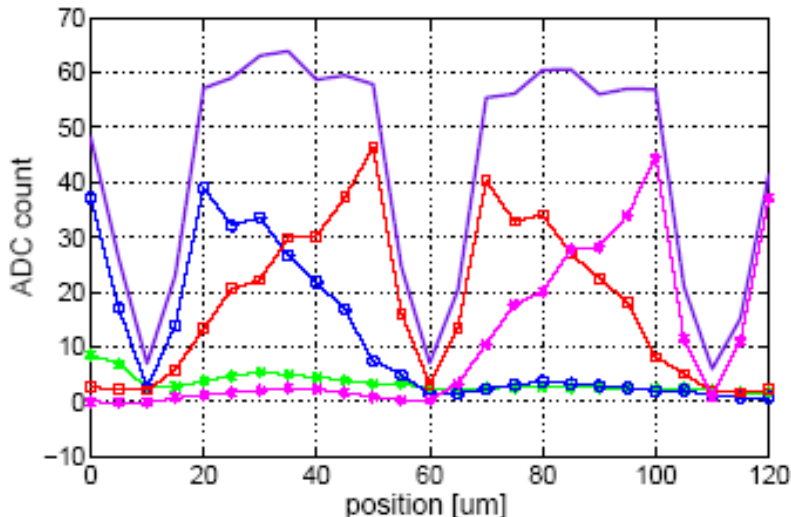


Figure 3: Typical response of a strip detector for a few channel where a laser moves across two strips in steps of  $5\mu\text{m}$ . The green line is channel 50, the blue line is channel 51, the red line is channel 52, and the pink line is channel 53. The purple line is the sum of all four channels

The mechanical aspect of thin silicon are frequently overlooked but they are equally challenging and will require as much time to develop as the sensors. There are three issues:

1. Acceptable yield
2. Handling post manufacture at HEP labs
3. Mechanical support

We address (2) and (3) here, the vendor is responsible for (1). We will produce thin silicon sensors which will be wire-bonded to existing electronics. These structures will be used with prototype mounting schemes. Full Finite Element Analysis models both mechanical and thermal will be developed. CTE mismatches are more serious for thin silicon sensors and so one example of the studies that will be performed is temperature cycling of the silicon, electronics and the mounting assembly. The mechanical studies will have an impact not only for microstrip sensors but also for CCDs, MAPS (Monolithic Active Pixels Sensors) and HAPS (Hybrid Active Pixels).

Finally, in parallel and in conjunction with other groups in the US, Asia and Europe we will study with Monte Carlo how to optimize the tracker design.

### Unique Facilities at Purdue

The proposed effort builds upon our experience in design and testing of silicon micro-strip and silicon pixels for CDF and CMS. We have access to CADENCE design tools and DESSIS simulation tools. The mechanical aspects of the project build upon our experience in the mechanical design, fabrication, and assembly of the silicon detector for CLEO III, and the mechanical design and prototyping of parts of the CMS forward pixel detector.

The detector facility at Purdue University, P3MD, contains two fully equipped clean rooms for the design, testing and assembly of detectors for High Energy Physics. These clean rooms

are part of a complex dedicated to microstructure detector development and fabrication including silicon strip and pixel devices and micro pattern gas detectors. The total clean room space is 3000 sq ft in three laboratories containing a CMM, wirebonder, electrical testing equipment, probe stations, optical tables, microscopes and high precision measuring devices. The labs are fully equipped with computer facilities for control, data acquisition and analysis. The labs have both temperature and humidity control and HEPA filtering of the airflow. Included in the clean rooms is additional space of class 1000. In a separate location there is a detector irradiation facility with an X-ray source and an ultra clean gas delivery system.

Other technical resources are also available, such as machine and electronic shops within the physics department, a central machine shop and state of the art facilities on campus, such as SEM, TEM (Transmission Electron Microscopy) and EDS (Energy Dispersive Spectroscopy). In addition to the technical staff, an engineer and technician, there is the normal complement of graduate students and research associates working on the Forward Pixel Detectors. There is also an exceptional pool of talented undergraduates who work on R&D and detector construction projects.

### **Results from Prior Research**

The Purdue group has considerable expertise in the development of silicon detectors. We played an important role in the design, installation and commissioning of the silicon vertex detector for CDF. The CLEO III silicon detector was built at Purdue. We are now playing a strong role for the CMS forward pixel project.

### **FY2006 Project Activities and Deliverables**

In the first year we will irradiate the sensors with x-rays and measure the DC properties of the sensors after irradiation. We will continue the studies of 300, 200 and 150  $\mu\text{m}$  thick sensors with the SVX4 chip before and after irradiation. The DAQ system is already operational. The measurements will be performed by a graduate student under the supervision of Petra Merkel who is already very experienced with this system.

We are also planning to participate in the simulation activities that are gaining momentum in SiD.

The deliverables in the first year will be a quantification of the importance of material minimization, based on more sophisticated MC studies, and an experimental measurement of the performance of thin sensors.

### **FY2007 Project Activities and Deliverables**

In the second year we expect to start studies of the mechanical mounting and the stability of thin silicon strips. There are several ladder designs that are under discussion within the SiD community. One achieves material minimization through a long ladder. The other relies on a short ladder design based on carbon fiber - rohacell support.

1. Studies of alignment and fabrication of low mass support frames will be conducted at Purdue. Metrology of thin silicon samples will be performed during cooling cycles. These will need to be conducted at cryogenic temperatures for CCD applications.
2. Finite Element Analysis (FEA) will be performed to understand the mechanical stability of thin silicon sensors and mechanical support structures.

The second year deliverable will be a systematic study of the mechanical issues associated with thin silicon strips.

Systematic studies will also be performed with the strips to determine the resolution and charge collection efficiency in a beam tests. Hopefully by that point an optimized LC readout chip might be available and a more realistic bench mark of thin silicon strip sensors will be performed.

The second year deliverables will be a first evaluation of the potential gain in resolution that can be achieved with thin, silicon sensors. We expect to perform:

- Beam tests for structures wire-bonded to electronics.
- Simulation of charge collection properties of structures, with both two-dimensional and three-dimensional simulation packages, CCE, pulse shape, operating conditions etc.

### **Budget justification:** Institution 1

We request funds to support 50% of a graduate student and a 50% of a postdoc. The remainder of the support for the student will come from the Purdue CDF group. The graduate student is charged at the rate set by Purdue University for 2006, increased by an estimated 5% per year thereafter. The remainder of the support of the postdoc will come from the Purdue CDF and CLEO groups. The postdoc and the graduate student will carry out the simulation studies and will evaluate the thin silicon sensors under the guidance of the senior personnel.

We request travel support for three trips each year to institutions working on LC vertexing. We are also asking for equipment items.

### **First Year Budget**

No equipment is required during the first year.

### **Second Year Budget**

The second year equipment budget will allow Purdue to build a system to study the mechanical issues connected with the thinning of sensors and readout chips. The study will include precision measurement of the stability of the support schemes as a function of temperature. Some of these studies will be conducted with blank silicon and some with functional sensors built using ADR funds. The graduate student at Purdue will work closely with the Purdue mechanical engineer (Kirk Arndt) to perform the temperature cycling studies. Thin sensors provided by ADR funding will allow a determination of the yield and the minimum thickness that is achievable by vendors.

Equipment breakdown:

#### **1. Precision alignment tooling: \$1.5K**

Vacuum holders for sensor/ROC assemblies and holders for support frames that precisely align the modules to the support frames. The cost is based on recent experience with similar tooling for CMS pixel R&D efforts.

#### **2. Fabrication and assembly of a low-mass support frame: \$2.2K**

The support frame will be either beryllium or carbon composite and will need to be of reasonably high precision.

#### **3. Thinned silicon, 2 batches @ \$1K per batch: \$2K (at no cost - ADR funding)** The cost estimate is based on previous purchases.

4. **Metrology: \$2.0K** This involves modifications to allow mounting of samples in a dry chamber which can be cycled to a low temperature. The modifications require an optical window to allow inspection and metrology during the temperature cycling. This will be similar to a chamber originally built by BTeV for their pixel studies but modified to allow for operation at cryogenic temperature for CCDs studies.

We also request funding to setup the beam test at Fermilab. This will include \$ 6.2 K to duplicate the PCI based DAQ:

1. **A dedicated PC: \$2500**
2. **PTA board** a PCI test adapter board based on the Altera FPGA Chip to interface between the PC and the PMC card: **\$ 1150**
3. **PMC a programmable mezzanine card** based on Xilinx FPGA Chip ro readout the ROC: **\$1150**
4. **2 power supplies: \$ 1400**

We anticipate using an already existng telescope at Fermilab to performe these measurments.

### Two-year budget, in then-year K\$

**Institution:** Purdue University

Item	FY2006	FY2007	Total
Post Doc (0.5 FTE)	23.1	24.3	47.4
Graduate Students (0.5 FTE)	10.3	10.8	21.1
Graduate Fee Remissions	2.75	2.89	5.64
Graduate Student Insurance	.47	.5	.97
Scientific Equipment	0.0	11.9	11.9
Travel	2.5	2.5	5.0
Indirect costs	20.3	21.3	41.6
Employee Benefits (Post doc)	9.47	9.96	19.43
Employee Benefits (Graduate)	0.041	0.043	0.084
Total direct and indirect costs	68.97	84.20	153.18

## References

- [1] M. Breidenbach, H. Weerts, J. Brau, and J. Jaros ,  
<http://www-sid.slac.stanford.edu/Documents/CriticalSiDQuestions.pdf>
- [2] Tesla, TDR, <http://tesla.desy.de/newpages/TDRCD/start.html>
- [3] The long shaping ladder option is described in Bruce Schumm's talk at the Victoria meeting. The short ladder option is described in Tim Nelson's talk at several SiD meetings.
- [4] S. Behari et al., CDF RUN IIB Silicon Vertex Detector DAQ Upgrade, Published Proceedings IEEE 2003 Nuclear Science Symposium (NSS) and Medical Imaging Conference (MIC), Portland, OR, October, 19-24, (2003).