

# STATUS REPORT

## Development of a Silicon-tungsten Test Module for an Electromagnetic Calorimeter

### Personnel and Institution(s) requesting funding

University of Oregon, Department of Physics and Oregon Center for HEP:

Jim Brau (faculty), Raymond Frey (faculty), David Strom (faculty), physics undergraduate(s)

University of California, Davis, Department of Physics:

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### Collaborators

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### Project Overview

The current LDC and SiD detector design concepts call for a silicon-tungsten (Si-W) electromagnetic calorimeter (ECal) as the best option for providing the necessary density and segmentation to implement the particle flow method (PFA) for reconstruction of jets (and taus) at the LC, capable of achieving jet energy resolution of  $\approx 0.3/\sqrt{E_{\text{jet}}}$ , as recommended by LC physics studies. One of the outstanding technical questions is how to integrate a silicon detector wafer with its readout electronics. Since the number of detector pixels for these ECal designs is on order 50 million, a solution to the integration issue, along with the cost of the silicon detectors themselves, is likely to determine the overall viability of the Si-W approach. A few years ago, we proposed [1, 2] a possible solution to the integration problem and have received LCRD support for three years to pursue this. The integrated approach also provides a design which naturally allows high transverse segmentation (currently 3.5 mm) and a small readout gap (currently 1 mm) to maintain a small Moliere radius.

During the past year we made important progress. The design of the readout chip (named KPjX) was completed and was sent to industry for prototype fabrication. This effort was led by SLAC. We have made progress characterizing the prototype silicon detectors at Oregon. A group at UC Davis has joined the effort and their budget request is included in this year's proposal. Davis has

developed a novel readout cable concept which will help maintain the thin readout gap. They will also will provide the bump bonding at Davis for the initial prototypes. Our work gives us confidence that we are on the right path and we propose for the next year to complete the initial phase of the R&D — to demonstrate the detector concept with prototypes in an electron test beam — and to move on to the next phase: The development of a full-depth ECal module which incorporates the features required for a realistic LC detector. This module could be part of an international test beam study. The full-depth module requires more funding than is realistically available with the present LCRD program. Hence, the required additional funding is being pursued separately. Here, we focus on completing the development and initial testing of the detector components, the goal being to test a few layers of our prototype detectors and electronics in the lab at Oregon and in an electron beam, hopefully at SLAC.

While we focus on an implementation of our Si-W approach for the SiD design, the basic ideas and R&D are certainly applicable to other Si-W ECal designs, notably LDC.

The thrust of our project is to integrate detector pixels on a large, commercially feasible silicon wafer, with the complete readout electronics, including digitization, contained in a single chip which is bump bonded to the wafer. The starting point for our design uses a pixel size of  $12 \text{ mm}^2$ , based on initial PFA requirements for photon-hadron separation. This gives  $N \approx 10^3$  pixels per 6-inch wafer. We take advantage of the low beam-crossing duty cycle ( $\sim 10^{-3}$ ) to reduce the heat load using power cycling. This scheme has several important properties:

1. The electronics channel count is effectively reduced by a factor  $N$ .
2. A transverse segmentation down to a few mm can be naturally accommodated.
3. The cost, to first order, will be independent of the transverse segmentation.
4. Readout gaps can be small ( $\sim 1 \text{ mm}$ ), thus maintaining the small Moliere radius intrinsic to tungsten.

The first property, we feel, is necessary for any realistic highly-segmented ECal. In this case, the electronics is likely to be relatively small fraction of the ECal cost. The third point makes the design flexible, so that one can optimize to meet the physics goals. The fourth is an optimization of the physics capability of the ECal at a given (barrel) radius. For example, the angle subtended by the Moliere radius for an ECal at radius 1.25 m with our design is smaller than one with 3mm readout gaps at 1.7 m. Hence, this has a significant impact on both performance and overall detector cost. We note that for a Si-W ECal, the features above remain unique to this R&D.

Our R&D collaboration has been holding weekly meetings by telephone for over three years. Although there is significant mixing, the responsibilities within the collaboration break down as follows:

SLAC: KPiX readout chip design, procurement, and testing.

Oregon: Silicon detector design, procurement, characterization, and testing.

Davis (new): Readout cable design and bump bonding of prototypes.

In addition, Veljko Radeka at BNL has provided critical advice and review of the electronics design and implementation plans. Recently, the Annecy group led by Yannis Karyotakis has begun working with us on the mechanical design, both for the prototype and for the final calorimeter. The funding for the Annecy R&D is being pursued separately. Oregon and SLAC plan to continue related simulation and software activities. These include, but are not limited to, EGS4 and Geant4 studies, comparisons between the two, and development of PF algorithms. Ultimately, we will use robust PFA results to optimize the calorimeter. This effort has strong ties to the Calorimeter Working Group of the ALCPG and to the Calorimeter group within SiD. We report regularly to these groups in regular telecons and at the workshops. Many of the details not presented here are collected at <http://www.slac.stanford.edu/xorg/lcd/SiW/> or in the cited references.

We are very aware of the separate Si-W ECal effort within the CALICE R&D collaboration. We note that the goals of the two efforts are considerably different. While we are pursuing R&D to develop detectors and electronics which we feel will closely resemble the final ECal, the CALICE effort has focused more on gaining experience with detector fabrication and in developing a working test beam module. In addition, the technical implementation of Si-W taken by the two efforts differs significantly. Since both of these approaches are important, it is premature, and probably counter-productive to merge efforts at this stage. In the meantime, we share our thoughts and concerns. The level of collaboration will increase as we approach full-module test beam studies. Following full-module tests, one expects the two R&D efforts to merge.

## Status Report

The most significant development for our project in 2005 was the completion of the design of the KPiX readout chip and the submission of the design to industry for fabrication of a first round of prototype chips to be tested. However, since no LCDRD funding is requested for this activity, we do not report on it here. A recent discussion of the KPiX functionality can be found in Ref. [3]. The following summarizes the progress during the past year on silicon detector R&D centered at Oregon and roughly follows Ref. [4]. This is followed by a discussion of the proposed R&D from the the UC Davis group.

### Progress at Oregon

In 2005 we continued measurements on the 6 inch Hamamatsu prototypes with particular emphasis on parameters relevant to use of the sensors with electronics designed for the cold ILC design. The most important measurements in this regard are the measurements of stray capacitance and leakage current. We have also investigated the use of a radioactive source for an absolute calibration. The results here are an update of our presentation[4] at LCWS05.

#### Pixel Capacitance and Trace Resistance

In almost all cases the noise of an individual pixel charge measurement in our detector will be directly proportional to the total capacitance seen at the input of the amplifier. The capacitance of a fully depleted 5 mm pixel in detectors 325  $\mu\text{m}$  thick, is expected to be approximately 5.3 pF.

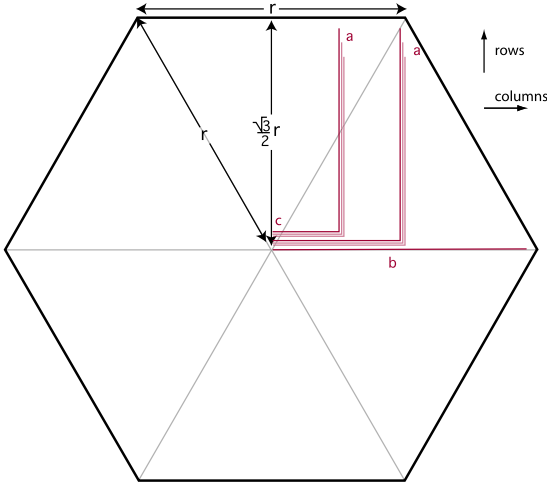


Figure 1: Example traces with varying amounts of stray capacitance. In the prototypes the  $r = 6.75$  cm.

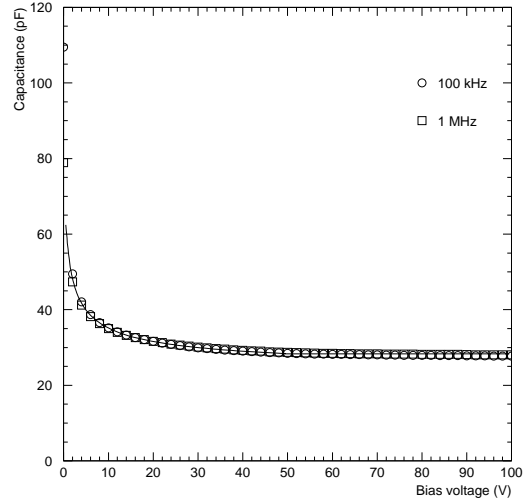


Figure 2: Typical capacitance versus bias voltage curve for a pixel located near region  $a$ .

The majority of the capacitance is due to the stray capacitance of the traces which connect the individual pixels to the bump-bonding array.

For the Hamamatsu process used in our detectors, the thickness of the oxide to the second metal layer is approximately  $0.9 \mu\text{m}$ . In our detector we used  $6 \mu\text{m}$  thick traces, giving a theoretical capacitance of approximately  $3.1 \text{ pF/cm}$ . The total amount of stray capacitance associated with a given pixel has two contributions. One contribution comes from the capacitance of the traces connecting the pixel to the bump-bonding array. The second contribution is due to any traces from other pixels which cross the pixel under test. The total stray capacitance is almost constant for many of the pixels as can be seen from Figure 1. In region  $a$  it can be seen that pixels located closer to the bump-bonding array have a greater number of crossing traces than those further away. This gives an almost constant total measured (and calculated) stray capacitance. Typical stray capacitances in region  $a$  were  $\sim 22 \text{ pF}$ . An example run is shown in Figure 2.

A small fraction of the pixels have a very large number of crossing traces. These pixels are located in regions  $b$  and  $c$  of Figure 1. For the first prototypes these pixels have capacitances of somewhat more than  $100 \text{ pF}$ . In a future version of the sensors we plan to reduce the stray capacitance in region  $c$  by narrowing the traces in the vicinity of the bump-bonding array. In Figure 3 the measured capacitances are shown for a large number of pixels in one quadrant for the Hamamatsu detector. In Figure 4 the expected capacitance for a future version of the detector with 1024 pixels and slightly smaller pixels is shown.

Another important property of the detectors is series resistance of the traces. The noise contribution from this series resistance is proportional to  $C_{tot} \sqrt{R_s}$  where  $C_{tot}$  is the total input capacitance

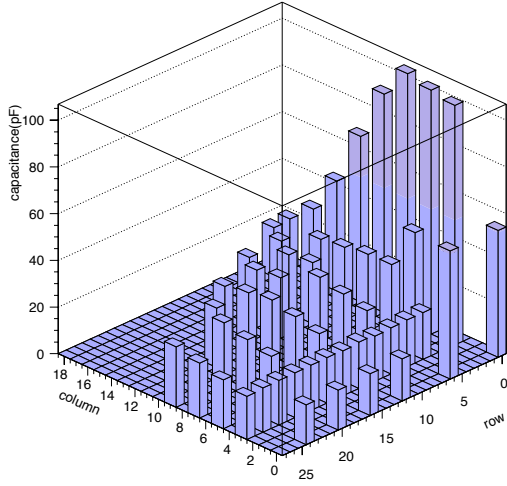


Figure 3: Left: Summary of capacitance measurements as a function of pixel position on the detector. The high capacitance of pixels at small row number is due to large number of traces in regions *b* and *c* of Figure 1.

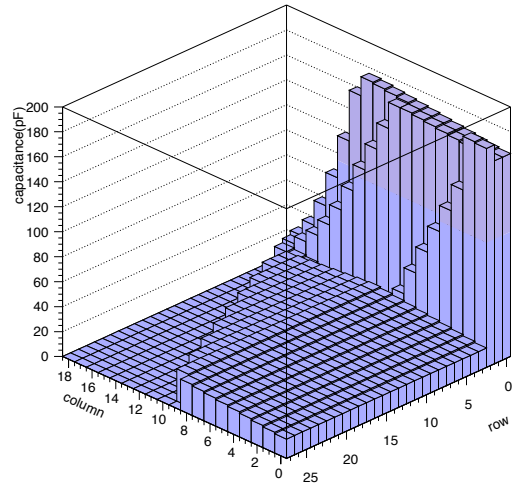


Figure 4: Expected capacitance in a 1024 pixel version of the silicon sensors with no change in pixel width from the current version. The current version of these detectors have 757 pixels and  $6 \mu\text{m}$  wide traces.

and  $R_s$  is the series resistance. The contribution to the noise from the input FET in a charge amplifier is proportional to  $C_{tot} \sqrt{\frac{2}{3g_m}}$  where  $g_m$  is the transconductance of the input FET. Thus it is desirable to keep  $R_s$  comparable to  $\frac{2}{3g_m}$ . In our case we expect  $\frac{2}{3g_m} \sim 300 \Omega$ .

Based on the measurement of one of the trace's resistance, we obtain a trace resistance of  $57 \pm 2 \Omega/\text{cm}$ . This can be compared to an expected value of  $47 \Omega/\text{cm}$  for a pure aluminum traces  $1 \mu\text{m}$  by  $6 \mu\text{m}$ . For the longest traces, of order  $10 \text{ cm}$ , the measured value implies a maximum resistance of  $570 \Omega$ .

It would be desirable to reduce this trace resistance by making thicker traces, however, it is unlikely that the thickness can be increased much beyond its current value of  $1 \mu\text{m}$ . Increasing the width of the trace is not helpful because it will increase the component of  $C_{tot}$  from the traces connecting the pixels to the bump-bonding array almost linearly. Except in the region the near bump-bonding array, our trace width of  $6 \mu\text{m}$  is close to optimal.

### Leakage Current

Leakage current can add an additional term to the electronic noise that grows with shaping time. Typical leakage currents in silicon pad detectors, such as the prototypes used here, have currents of a few  $\text{nA}/\text{cm}^2$ . The leakage current was measured during the capacitance tests and was found to be less than  $2 \text{ nA}/\text{pixel}$  for pixels in the interior of the detector. In our tests the neighboring pixels

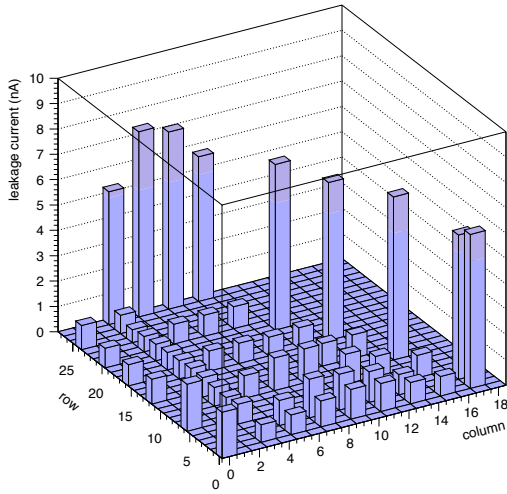


Figure 5: Left: Summary of capacitance measurements as a function of pixel position on the detector. The high capacitance of pixels at small row number is due to large number of traces in regions *b* and *c* of Figure 1.

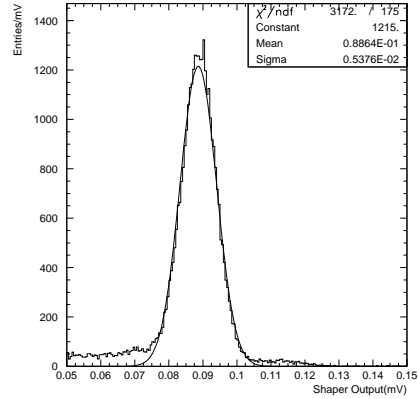


Figure 6: Signals from Am<sup>241</sup> 60 keV photons observed in a typical Hamamatsu silicon sensors pixel.

and the guard ring were left “floating” . For pixels on the edge of the detector, with the guard ring floating, the leakage current was less than 10 nA/pixel, see Figure 5. We expect the noise contribution for leakage current to be minimal; the expected contribution for a leakage current of 10 nA and an integration time of 1  $\mu$ s is only 250 electrons.

### Calibration

Calorimeters based on silicon are expected to be quite stable over time. The largest changes in calorimeter response will be due to changes in the electronics. The readout electronics are being designed with an internal calibration system that allows a wide variety of charges to be injected into each of the channels in the system. The accuracy of this system is expected to be limited by the knowledge of the values of the coupling capacitors incorporated into each of the channels in the readout chip. These capacitors are expected to be uniform, within a chip, with a spread of  $\sim 1\%$ . This spread is unlikely to have a noticeable contribution to the energy resolution of the calorimeter. Chip-to-chip variations could be larger.

One possibility is to calibrate each sensor after the readout chip has been bump bonded. A possible method for this calibration would be to use 60 keV photons from the decay of radioactive Am<sup>241</sup>. If the energy from these photons are fully contained in the silicon sensors they will give

a signal of approximately 16,000 electrons. This is somewhat less than the MIP signal, but well above our noise floor.

The 60 keV photons will easily penetrate any mounting structures and printed circuit boards used in the testing and assembly of the calorimeter. However, the calibration must be done before the detector assemblies are placed between the tungsten sheets, as the photons will not efficiently penetrate the tungsten. We have used our laboratory electronics to measure the energy spectrum from the Am<sup>241</sup> photons in the pixels as shown in Figure 6. The widths of the peak is consistent with the expected electronic noise.

As a demonstration of this technique we show the value of the photon Am<sup>241</sup> peak versus pixel capacitance in Figure 7. The peak shifts to lower values at large values of the capacitance because of the finite input capacitance of laboratory electronics. The line corresponds to a ‘dynamic’ capacitance of our laboratory electronics  $C_{dyn} \sim 790$  pF which is consistent with the laboratory amplifier’s specifications.

In the readout chip planned for the final detector, the signal-to-noise for Am<sup>241</sup> peak will be about 8, which will broaden the peak considerably. Another important aspect of the planned readout electronics will be that a measurement of the charge will be done relative to an external bunch clock rather than relative to the time of arrival of the photon as was done in the laboratory. This will lead an additional smearing of the observed spectrum of less than 5%. Thus we expect a total width for the Am<sup>241</sup> 60keV signal of approximately 15%.

The ADC in the planned detector readout will have a least significant bit approximately equal to the expected noise. Therefore, if there were no systematics in the ADC it would be possible to calibrate each pixel to 1% with approximately 250 detected photons. For this calibration to be useful it will be necessary to relate the charge scale at 8 ADC counts to that at full scale readout. This is possible, but will require great care in the design of the calibration circuit on the readout chip.

Somewhat easier, but still difficult, will be a wafer-to-wafer calibration at the sub-percent level. Here one can average over 1024 pixels/wafer. Again it will be necessary to relate the average charge scale at 8 ADC counts to the average full scale readout.

### Cross Talk

We are continuing to study cross talk introduced by capacitive couplings between the channels. In general these have lead to cross talk at the 1% level or below. The cross talk is function of both the capacitive coupling and the properties of the readout electronics. While we have a qualitative understanding of the cross talk, we are continuing to work on a quantitative model and on incorporating the properties of the KPiXs electronics into the model.

### **UC Davis Proposed R&D**

The device discussed above consists of interspersed layers of a radiator (W) and a sensor (Si) which together form a sampling calorimeter. The sensor layer is composed of a set of hexagonal silicon diode wafers tiling the surface of a large W panel. Each wafer is divided into pixels, the pickup

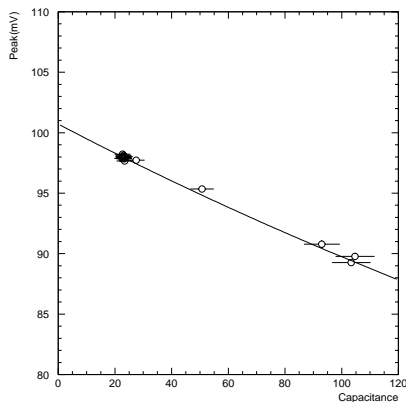


Figure 7: Measured position of peak versus total pixel capacitance.

pads of which are connected by traces to an array of contact pads. The ASIC readout chip contains unit cells of electronics arranged in an array that matches that on the wafer. The connections between the array of sensor pixel traces and the array of readout cells are made by flip chip bump bonding of the ASIC to the sensor wafer. Communications between the ASIC and the readout system located at the periphery of the calorimeter are also accomplished via pads located on the sensors. These pads will connect with buses made out of flexible kapton cables. UC Davis will carry out the following tasks:

Bonding of readout chips to the sensor wafers. To do so, we will use photolithography techniques to form the appropriate array pattern in the center of a sensor wafer. In a separate process, a readout chip will have a similar pattern placed on it. Under-bump metallization will be sputtered onto each array. This will take place in the Microfabrication Facility on the Davis campus. Indium will then be evaporated onto the wafer and also onto the readout chip in our own physics laboratory. After liftoff of the photoresist, the wafer and readout chip will have on them matching arrays of indium bumps. The flip chip bonding will then take place using a Research Devices M8HP bonder at UCD. Here, the two indium arrays are precisely aligned in the bonder and pressed together to form a cold weld of indium to indium. The process will be repeated for many wafers and chips, and the result will be a set of sensor/readout units that will be used to tile the SiW layer. We have used this procedure for many individual readout/sensor bondings, in particular for all of the prototype CMS Forward Pixel Detector units. Indium bonding is also being used by the Paul Scherrer Institute group for the CMS barrel pixel detector.

Design and Fabrication of flexible cables. The array of sensor plus readout chip units in a given layer will need to be controlled and read out by electronics that will reside on the periphery of that layer. In order to achieve the best possible energy resolution in the calorimeter, the gap between layers needs to be minimized. The present design calls for a gap thickness of 1 mm or less. We are proposing to use a flex cable technology for the data and control bus and some form of bump

bonding to connect the cable to pads located on the silicon wafer substrate. The cable will most likely be at least 4 layers with 2 shielding/power layers and vias that connect to traces running along 2 buried layers. A need for placing bypass capacitors on the cable is also foreseen if they can be accommodated without increasing the overall thickness substantially. We will design this cable at UCD using the Mentor Graphics/PADS software package and have them fabricated by an outside vendor. The testing of the cable will take place at UCD using our probe station. The group has fabricated a similar cable for the CDF experiment and has experience in designing dozens of circuits using PADS.

#### **FY2006 Project Activities and Deliverables:**

- Receive KPiX prototype chips and evaluate functionality (mostly at SLAC).
- Complete evaluation of first round of prototype detectors (Oregon).
- Develop and fab. first kapton flex readout cable (Davis).
- Design 2nd round of detectors to be used in full ECal module (Oregon, SLAC, Davis).
- Design concentrator boards (digital boards downstream of KPiX) (SLAC).
- Prepare for mounting of 1st round KPiX prototypes to 1st round detectors (Davis, Oregon, SLAC).
- Mount (bump bond) about 10 KPiX to detectors (Davis).
- Develop mechanical design for full ECal module (Annecy, SLAC, Oregon).

#### **FY2007 Project Activities and Deliverables**

- Carry out full tests of a few layers in lab and electron beam at SLAC of KPiX-detector prototypes (Oregon, SLAC, Davis).
- Mount (bump bond) KPiX to 2nd round detectors for ECal full module (Davis).
- Carry out mechanical and magnetic field tests of KPiX + detectors (Oregon, Annecy, SLAC).
- Order full 1024-channel KPiX chips (SLAC).
- Fabricate full ECal module (all).
- Put full module in electron beam at SLAC for determination of EM response and resolution (all).

We are considering as many as three beam tests. The first is a “technical” test (early FY2007) of 1-2 layers (i.e. one layer  $\equiv$  one detector with one readout (KPiX) chip). Next, we would test the full-depth ECal module in an electron beam, presumably at SLAC, to fully map out electromagnetic response and resolution. Hopefully, this will occur in FY2007. Finally, we would put our module plus an LC HCal module into a hadron beam, probably at FNAL, to determine hadron response and validate the GEANT4 simulation codes upon which the design of a full detector relies. There are currently several possible scenarios for this test. The validation of the simulations will presumably be aided by using detectors (ECal and HCal) with fine segmentation, hence there would be an important role for our module in such tests.

Taking into account damage, lab tests, and so forth, we will need to procure about 40 new silicon detectors for the full-depth ECal module. We estimate the cost, based on our previous order, to be about 200k\$, about 35% of which would be NRE for the photomasks. Hence, Oregon is seeking 50k\$ over two years in this proposal and the remaining 150k\$ outside of the LCDRD process.

In the following, we present the Oregon budget and justifications, then the Davis budget and justifications, followed by the total project budget.

**Oregon Budget justification:**

We request lab test equipment and supplies, partial funding for prototype detectors (see discussion above), and undergraduate wages to carry out our program.

As discussed above, we request a total of 50k\$ over two years for the detectors for the full module. This is to be supplemented by 150k\$ requested separately.

For the technical beam test we request 5K\$ for the design and fabrication of mechanical fixtures.

Lab test equipment request includes the following: Low and test amplifiers (2k\$), clean room supplies (2k\$), and an FPGA card (2k\$) for the back-end readout.

For the development of our printed circuit motherboard for the first beam test we request 4k\$ for its design, 4k\$ for its fabrication, and 2k\$ for the required wire bonding to the KPix chip. Note that the Davis flex cable will eventually replace functionally replace this.

Travel includes test beam related shipping in addition to some travel to LC workshops.

We currently employ an equivalent of two undergraduate physics students in our R&D at the level of 10 hours per week. We request support for 40 weeks per year of support for each of two students, at hourly wages of \$8/hour with no fringe benefits. Including indirect, this is about 10 k\$ per year.

The indirect rate is 26%. Indirect is not applied to equipment for items costing more than 5k\$. So we assume no indirect is applied to the silicon detector orders. Otherwise, the numbers given above include indirect, so are 26% larger than the ones in the table below.

The item for PC board development included in last year's proposal, is now, in part, transferred to UC Davis under flex cable development.

**Oregon two-year budget, in then-year k\$:**

Item	FY2006	FY2007	Total
Other Professionals	0	0	0
Graduate Students	0	0	0
Undergraduate Students	8.0	8.0	16.0
Total Salaries and Wages	8.0	8.0	16.0
Fringe Benefits	0	0	0
Total Salaries, Wages and Fringe Benefits	8.0	8.0	16.0
Equipment	30.5	29.7	60.2
Travel	1.6	1.6	3.2
Materials and Supplies	0.8	0.8	1.6
Other direct costs	0	0	0
Total direct costs	40.9	40.1	81.0
Indirect costs(1)	4.13	3.93	8.06
Total direct and indirect costs	45.03	44.03	89.06

**UC Davis Budget justification:**

For the bump bonding and flex cable development, we will need two technicians (0.25 FTE each). The expertise required for the two tasks is vastly different and it is unlikely that one Tech would be trained in both. Based on present experience, the personnel costs, spread over the two years, are estimated to be 8.0k\$ for the bump bonding (at 0.25 FTE) and 12k\$ for the flex cable (at 0.25 FTE). Fringe benefits are included in these figures.

We assume that there will be 40 wafer/readouts to be bonded during 2006-07. These could be arranged in one tower 30 layers deep and also, in two strings of 10 wafers that will test the layer readout design. For the purpose of this budget, we assume only 10 wafers will be bump-bonded in 2006. The bump bonding effort over the two years includes supplies (photoresist, indium, miscellaneous): \$2,000; Microfab Facility charges: \$5,600; Ti/W sputtering target: \$850. The microfabrication facility at UCD charges \$28/hr with a maximum of \$2,800/month once the usage exceeds 100 hours. We estimate 1 day/chip for patterning, for a total of 30 days, which can not be accomplished in one month. Hence, we have budgeted for a total of 2 months of usage of the microfab facility.

The NRE estimate for the flex cable is \$2,800, based on actual quotes obtained from a vendor based on a preliminary design that contained all the required features but not the ultimate complexity of the design. We anticipate two rounds of prototyping in order to produce the final version of the flex cable. The actual fabrication cost is estimated at 1.0k\$. We envision two rounds of design and fabrication, giving a total of about 8k\$.

The indirect rate is 26%.

**UC Davis two-year budget, in then-year k\$:**

Item	FY2006	FY2007	Total
Other Professionals	9.0	11.0	20.0
Graduate Students	0	0	0
Undergraduate Students	0	0	0
Total Salaries and Wages	9.0	11.0	20.0
Fringe Benefits	0	0	0
Total Salaries, Wages and Fringe Benefits	9.0	11.0	20.0
Equipment	3.8	5.0	8.8
Travel	2.0	2.00	4.00
Materials and Supplies	1.85	1.0	2.85
Other direct costs	1.6	4.0	5.6
Total direct costs	18.25	22.0	40.25
Indirect costs	4.745	5.720	10.465
Total direct and indirect costs	22.995	27.720	50.715

**Combined Oregon and Davis totals, in then-year k\$:**

Item	FY2006	FY2007	Total
Total direct costs	59.15	62.10	121.25
Indirect costs(1)	8.88	9.65	18.53
Total direct and indirect costs	68.0	71.7	139.7

## References

- [1] M. Breidenbach, talk at Chicago LC Workshop, Jan. 2002, <http://LCworkshop.uchicago.edu/>; updated at Cornell workshop, July 2003, <http://www.lns.cornell.edu/LC/workshop/>.
- [2] R. Frey, talk and proceedings paper from Calorimeter 2002, Pasadena, CA, March 2002, documents available at <http://3w.hep.caltech.edu/calor02/> ; talk presented at Linear Collider Workshop, LCWS2002, Korea, Aug. 28, 2002, <http://lcws2002.korea.ac.kr/>.
- [3] M. Breidenbach, talk presented at LCWS, Stanford, CA, March 2005. See URL: <http://www.pd.infn.it/~chechia/lcws05/SID.ppt>
- [4] David Strom, talk presented at LCWS, Stanford, CA, March 2005. See URL: <http://www.pd.infn.it/~chechia/lcws05/strom-cal.pdf>