

PROJECT DESCRIPTION

Project Name

Real Time Simulator for ILC RF and CryoModules

Personnel and Institution(s) requesting funding

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Anna Grassellino (1st year graduate student) University of Pennsylvania
Justin Keung (1st year graduate student) University of Pennsylvania
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Collaborators

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Project Leader

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Project Overview

We propose to develop a detailed real time simulator and simulation package to model the behavior of an ILC RF unit. An ILC unit is presently defined to be 24 cavities distributed in three cryomodules with RF power. The high operational overhead and potential risk of damage during tests of control hardware makes it important to develop a realistic test bed independent of the cryomodules and associated RF hardware. We are using the simulation package to understand and redefine in some cases, the specifications for the RF and LLRF system for the ILC BCD. This work has begun and we report some preliminary results later. We plan to move the simulation package into a hardware implementation, such that we can have a real time simulator (RTS) of the RF unit and cryomodules. Based on discussions with RF and LLRF colleagues at Fermilab, Ruben Carcagno, Brian Chase, Gustavo Cancelo, and Sergei Nagaitsev, we will implement the RTS package using a common simulation toolset based on the MATLAB symbolic simulator, Simulink, and a commercial digital communications board. We have had discussions with colleagues at Pisa (Fabrizio Scura) and DESY (Elmar Vogel and Stefan Simrock) and are exploring a possible collaborations with them. This project is aimed initially at the Fermilab ILC beam test facility, but will also be of use to RF and cryomodule testing facilities at DESY and KEK as well. The RTS will be used for testing and commissioning of the Low Level RF control, exception handling, and possibly as a noiseless behavioral reference for each cryomodule during operation.

Broader Impact

This proposal will train accelerator physicists. There are already two graduate students (one of whom is a woman) involved and interested in careers in accelerator physics. There are two undergraduates working on the project for the summer.

Results of Prior Research

The Penn group has been developing a SRF cavity simulator for about six months. In addition, we have been interacting with the international LLRF community for over one year and we have participated in “LLRF week” at DESY in the TTF test beam.

Effects included in the present version of the simulation are:

1. cavity detuning
2. Q-drop and Q-slope
3. phase noise (phase jitter)
4. beam loading
5. feedback gain and loop delay (gain bandwidth product)
6. electronics and cable feedback delay
7. klystron power saturation (CPI)
8. modulator ripple (MARX and Fermilab modulator power shapes)

A detailed description of the simulation exists and is available at Justin Keung’s web page (<http://einstein.hep.upenn.edu/~keungj>). Instructions are provided on this web site for running the simulator and results on each of several study topics are presented in a short note format. Notes available include: Full Design Note for Cavity Simulation, Effects of the Q of Cavity on Amplitude and Phase Noise, Effects of Noise versus Varying Feedback Gain, and Effects of the LLRF Control Latency.

The cavity model has been implemented in “C” code and is based on the observation that to first order a cavity behaves like an elementary R-L-C network as presented in the 1998 Thesis of Schilcher [1]. As with any R-L-C circuit, the voltage and current behaviour can be modeled by a set of differential equations. Lorentz force de-tuning [2] is added as a refinement of the cavity behavior and the non linear effects of the klystron drive were added as first order improvements on the model. We have used it to look at the effects of loop delay, clock jitter, and modulator ripple on feedback for the LLRF control. Feed Forward algorithms are now being examined.

As an example of a test run of the cavity simulator, we show results for amplitude and phase response of the Tesla cavity. Figure 1 shows two plots that indicate the accelerating gradient filling time, flat top, and decay, the effects of Lorentz Force detuning and the varying Q of the cavity and the beam loading. The changing phase, which agrees well with TTF test beam behavior is shown in the second plot.

Facilities, Equipment and Other Resources

The Penn High Energy Physics group is well supported by DOE HEP. It is one of the stronger university instrumentation groups in the country. The group designs custom integrated circuits and has provided integrated circuits to many groups around the world as a by product of our own program, at cost. The ASDQ chip, used for drift chamber readout, is one example. It is the frontend readout chip for the CDF Central Outer Tracker(30,240 channels), that was Lockyer and Newcomer’s main responsibility to the CDF upgrade. We design and build complex circuit boards, program FPGAs, and design numerous electronic systems. The group has just finished delivering 375,000 front-end readout channels for the Atlas Transition

Radiation Tracker. Penn has excellent computing available and substantial lab space for the HEP group.

First year Project Activities and Deliverables

Symbolic Device Blocks

We propose to develop an ILC specific library of symbolic library blocks that model specific physical objects in the accelerator system: Klystron, Modulator, Cavity, etc. These symbolic blocks would employ a 'C' based representation for software modeling and an 'HDL' based model for hardware response representation. The Block format would allow for 5 basic parts although the HDL model would only be used where a hardware output was directly or indirectly involved.

It has been shown by E. Vogel and W. Hofle [4] that accelerator components can be successfully modeled using a MATLAB based symbolic representation tool called Simulink. Their work on the CERN SPS beam was able to predict residual transverse oscillations in a stored beam bunch due to the extraction of a previous beam bunch. As a result a model for a transverse feedback system was developed and will be used to damp the beam in the SPS ring.

ILC specific Symbolic Blocks that we and others develop would be reviewed by institutions with expertise in the appropriate areas such as (DESY, PISA, Fermilab, SLAC, KEK) and "registered" when consensus is reached on their fidelity. In this way both baseline and proposed hardware could be modeled. LLRF control algorithms could be tested and device specific specifications could be proposed before the hardware was available for integration into a beamline.

Real Time Simulator

We propose to extend the software representations of the cavity and high level RF system into a Hardware based Real Time Simulator (RTS). We have identified commercially available high speed hardware (LyrTech VHS-ADC) with multiple A/D and D/A's and a very large FPGA on a single board. The board has a latency for a simple R/W cycle of less than 200 ns from A/D input thru the FPGA and out to a D/A. With this board, a real time response appears to be within reach. We would develop the RTS in steps:

1. A single cavity model with IF Vector Modulator inputs (driven by the LLRF control) and three IF output mimicking the downconverted field pickup signals. This model would immediately allow for several interesting tests to be performed with any LLRF controller. For example: Noise can be added to the IF output to understand how to cope with noise in the down convertor and klystron performance characteristics such as saturation and power variation due to modulator ripple can be added.
2. A multi-cavity module can be modeled by phasing the RF from each of the cavities by the appropriate phase. Since the LyrTech board has only 8 D/A outputs a second daughter board with up to 16 D/A's would be required if more than one output per cavity is required.
3. The ultimate goal would be to model a full ILC RF unit consisting of three 8 cell cavities powered by a single klystron and modulator. The phasing of the output IF between boards will be critical. The LyrTech 400MHz front panel data port will allow fast updating to multiple boards.

At any stage additional quality monitor outputs may be added. Beam quality monitors, modulator ripple monitor, microphonics monitors etc. The bandwidth and latency of these inputs would play an important role in determining how they were included in the system.

The RTS engine, LyrTech VHS-ADC Board

The engine of the RTS is the LyrTech VHS-ADC Board (see appendix 1 for a more complete description). The VHS-ADC board has 8 channels of D/A that can operate at 125 MSPS and 8 channels of A/D that can be added via daughter board that can operate up to 105 MSPS. These speeds should be high enough to allow for an IF frequency of up to 52.5 MHz. Output waveforms will be driven by an Xilinx Virtex II - 6000 with 6 million gates. An internal or external clock can be used to drive the D/A, A/D and FPGA clocked operations. The board includes a front panel Data Port with up to 400 MBytes per second data transfer rate to keep other boards updated. In addition, very fast I/O can be performed by a General Purpose I/O output driven directly by the Virtex II. It can be programmed to have up to 6 LVDS pairs, each operating at 800Mbits/sec. The VHS-ADC will require a c-PCI crate and PC interface. We will also need low and high level firmware (MATLAB/SIMULINK) drivers and software support from LyrTech. As we move from a single cavity simulation to a full ILC RF unit with one klystron and three cryo-modules, we will need additional D/A outputs. A single 4 slot crate c-PCI bus can support three LyrTech boards, 48 high speed channels of D/A and A/D that may be split into 8 channel increments. The total number of fast outputs per cavity is not yet fully defined. Assuming that only the RF field probe measurements need to be updated at the IF rate, then the 40 possible D/A outputs in a 4 slot PCI crate should be sufficient. Additional A/D or D/A outputs would require an expansion crate.

The RTS will make it possible to evaluate RF control elements without attaching to an actual cavity. Effects of heating, beam transmission and noise can be included. The IF output signals per cavity provided by the “final” RTS will include RF field from the cavity as well as transmitted and reflected power from the cavity coupler. More signal outputs are possible as we learn what is valuable to use to keep the LLRF updated. In addition, exception handling may be better understood to help minimize the beam turn on time and reduce down time due to mistakenly identified fault conditions. RF element failures may be simulated and their warning signs may be identified by limiting the non ideal behavior of other parts of the system. The synchronous RTS operation of a full ILC RF unit (1 klystron and 3 modules) will allow us to learn the sensitivities of Feedback and Feed Forward algorithms as well as to test recovery modes from various hardware parametric changes. Clearly there will be significant learning advantages both planned and unforeseen with a working RTS.

Year One Deliverables

1. implement a multi-cavity simulation and include coherent and incoherent effects
2. include beam amplitude jitter, noise, and temperature effects in the simulation
3. determine the gain and latency needed for the ILC feedback LLRF system.
4. determine the tolerance specification for the modulator power ripple
5. Implement an IF measurement and control based Symbolic Cavity Block, with RF phase and amplitude inputs coupled in from the Klystron, and three output parameters, input and reflected power, and RF field from the cavity in Simulink.
6. Purchase Hardware with 1 VHS-ADC board for a Single Cavity Simulator and develop a first level Real Time Cavity, Simulator.

7. Measure and compare the performance of a real single cavity to the simulation.

The simulation improvements and process for tolerance specifications will be completed by December 2006. The RTS will be implemented by summer 2007.

Second year Project Activities and Deliverables

Year Two Deliverables

1. Evolve the single cavity RTS and Symbolic Cavity Blocks to the cryomodule and RF unit level.
2. Purchase additional D/A boards as required with attention to required bandwidth.
3. Test outputs against real cavity signals.
4. Implement RTS with the LLRF control system or systems being designed elsewhere.

We expect that there will be a continuous evolution of the RTS and symbolic block device representations once cryomodules are available.

Budget justification: University of Pennsylvania

The budget supports one postdoctoral fellow, two summer stipends for graduate students, two undergraduates for the summer, and travel. The travel consists of 2 international trips per year for Lockyer, Newcomer, and the postdoc. It also includes trips to Fermilab once every two months for the postdoc, one every two months for Newcomer, and once every 3 months for the graduate students. As a reference Justin Keung, even though taking classes, has traveled to Fermilab twice in the last two months for workshops and presentations. We expect this to continue, but cannot continue using CDF funds. His presentations can be found on the WEB page sited above for the simulation. The students are supported by the university during the 9-month school year as teaching assistants. Lockyer travels to Fermilab by combining all trips with CDF activities.

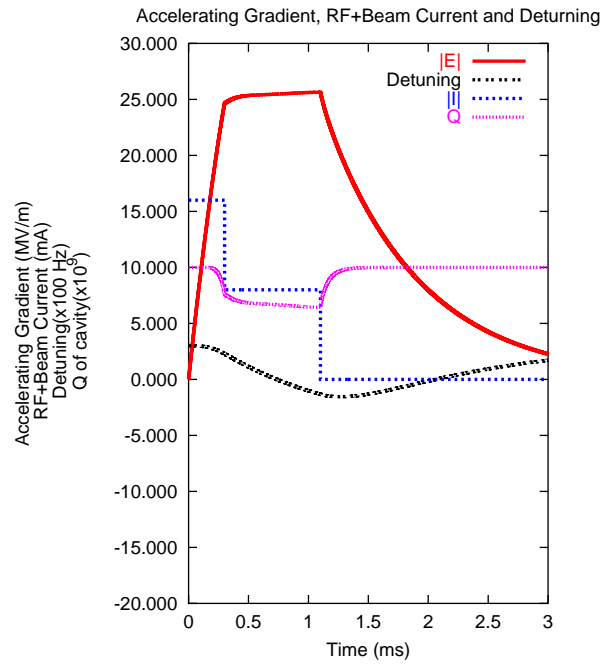
The hardware, described above, consists of a 4-slot c-PCI crate, a processor board and the FPGA board with D/As and A/Ds. In addition, the full suite of simulink software is included and the quotation includes a significant educational discount of \$10,111 applied to the hardware and software. In addition, annual cost for the MATLAB environment software with components for RF control is \$2800 per year. We are attempting to get an additional discount through the university. Hardware and software costs are \$25,870 in the first year. In the second year, we purchase two additional D/A boards each \$11,900, Lyrtech driver software maintenance for \$800, MATLAB environment \$2800, for a total of \$27,400.

The fringe benefits are employee part-time benefits of 5005 year one and 5155 year two. Health insurance for the postdoc is \$6000 year one and \$6180 year two.

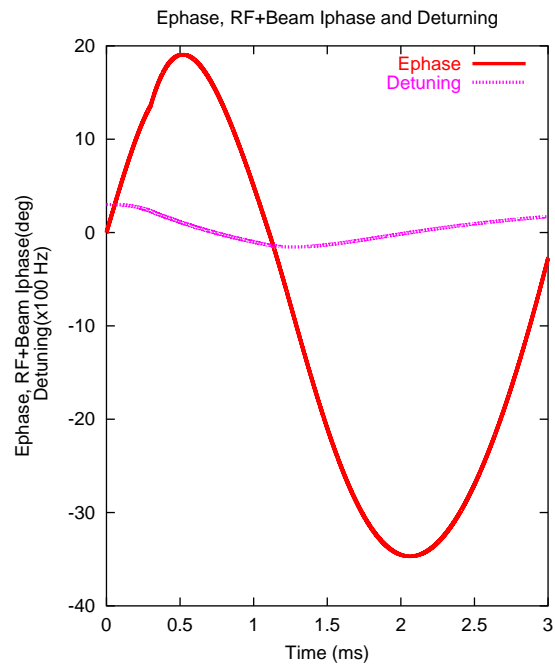
The budget has been prepared in accordance with University of Pennsylvania overhead and employee benefit rates.

Institution: University of Pennsylvania

| Item | First year | Second year | Total |
|---|------------|-------------|--------|
| Other Professionals(PD) | 42000 | 43260 | 85260 |
| Graduate Students | 11072 | 11404 | 22478 |
| Undergraduate Students | 9600 | 9888 | 19488 |
| Total Salaries and Wages | 62673 | 64553 | 127226 |
| Fringe Benefits | 5005 | 5155 | 10161 |
| Total Salaries, Wages and Fringe Benefits | 67678 | 69708 | 137386 |
| Equipment | 25870 | 27400 | 53270 |
| Travel | 21000 | 21630 | 42630 |
| Materials and Supplies | 0 | 0 | 0 |
| Other direct costs | 6000 | 6180 | 12180 |
| Institution 2 subcontract | 0 | 0 | 0 |
| Total direct costs | 120548 | 124918 | 245466 |
| Indirect costs(1) | 53966 | 56073 | 110039 |
| Total direct and indirect costs | 174514 | 180991 | 355505 |



(a) Amplitude response



(b) Phase response

Figure 1: Cavity response of a real niobium cavity, with initial +300 Hz detuning .

References

- [1] Thomas Schilcher, *Vector Sum Control of Pulsed Accelerating Fields in Lorentz Force Detuned Superconducting Cavities*, Dissertation zur Erlangung des Doktorgrades des Fachbereichs Physik der Universität Hamburg , Hamburg (1998), Ch.3 and Ch.6.
- [2] A. Mosnier, *Dynamic Measurement of the Lorentz Forces on a MACSE cavity*, DESY Print TESLA 93-09 (1993).
- [3] Wenzel Associates Inc., <http://www.wenzel.com/documents/noise.html>
- [4] W. Hoffe, E. Vogel, *Simulation of Transient Effects of Beam - Transverse Feedback Interaction with Application to the Extraction of the CNGS Beam from SPS*, CERN-AB-2005-010.