Design and Fabrication of a Radiation-Hard 500-MHz Digitizer Using Deep Submicron Technology

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Project Summary

The proposed International Linear Collider (ILC) will use tens of thousands of beam position monitors (BPMs) for precise beam alignment. The signal from each BPM is digitized and processed for feedback control. The demand on the digitizers depends on their location at the accelerator complex. The two large damping rings require the fastest high-precision and high-bandwidth digitizers. We propose to continue the development of the digitizers that were originally designed for the warm linear collider. The specification of the digitizers for the ILC is not yet finalized but we expect similar digitizers are needed.

We propose to continue the design of an 11-bit (effective) digitizer with 500 MHz bandwidth and 2 G samples/s. The digitizer is somewhat beyond the state-of-the-art and hence not commercially available. Moreover we plan to design the digitizer chip using the deep-submicron technology with custom transistors that have proven to be very radiation hard (up to at least 60 Mrad). The custom enclosed layout transistors with guard rings were developed for high-energy physics applications in very high radiation environment. The design mitigates the need for costly shielding and long cable runs while providing ready access to the electronics for testing and maintenance. Once a digitizer chip has been successfully developed via several prototype runs, an engineering run at a cost of ~$150,000 will produce all the chips necessary for the ILC, including those BPMs that require less demanding digitizers. We have extensive experience in chip design using Cadence3. This proposal was reviewed by the Holtkamp Committee in 2002 and 2003 and awarded, for both years, a rank of 2 on the scale of 1 to 4 with 1 having the highest ranking. This proposal was funded by DOE in FY03 and has been reviewed for three more years, FY04-6. Most of the circuit blocks in the chip were designed and simulated in FY04. For FY05, we concentrated on the most crucial component of the digitizer, sample/hold circuit, and achieved a precision of 10 bits. We plan to continue to improve the precision to at least 11 bits before submitting the first prototype chip for fabrication in FY06. This represents a delay in the submission of the first prototype fabrication. However, given the cost of fabrication, we believe that it is more sensible to prototype a chip that is closer to the design specification. We request continue funding for FY06 and FY07 to continue the design work and submit the second prototype chip in FY07 to evaluate and improve the design.

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Project Plans

The digitizer chip is very challenging: large bandwidth (500 MHz), high precision (11 bits), and fast sampling speed (2 G samples/s). We capitalize on the experience of our engineering staff that, over the last ten years, has designed radiation hard chips for ATLAS, CLEO III, and CMS. Our most recent design of the DORIC and VDC chips for the ATLAS pixel detector uses the IBM deep submicron technology with feature size of 0.25 µm to achieve radiation hardness. In addition, we have extensive experience designing fast analog electronics systems such as those used in high-resolution drift chambers.

We propose a 12-bit pipelined digitizer as shown in Fig. 1. In this scheme the input is crudely digitized in the first stage (3-bit cell). The digitized value is then subtracted from the sampled input value, amplified by eight and presented to the second stage. This identical process is repeated for each of the four stages. A one-bit comparator follows the last stage so the final result can be rounded to 12 bits.

The 12-bit digitizer is somewhat beyond the state-of-the-art. However, there is one characteristic of the BPM that may ease the design requirements. The input from each bunch to this system is a sequence of doublets. We currently design the digitizer for a bunch spacing of 1.4 ns. The bunch spacing is expected to be somewhat larger for the dumping rings of the ILC and this will improve the feasibility of the project. Only one parameter is needed to completely specify a doublet. Thus the requirements could be met with a digitizer sampling at the bunch frequency (1/1.4ns or 714 MHz). By interleaving three digitizers, we can have a chip with 2 G samples/s to provide more redundancy. In the following, we first discuss the required precision of some of the circuits in the digitizer and then the control of the errors in order to achieve the desired precision.

![Figure 1. Schematic of a 12-bit pipelined digitizer.](image)

Precision

Submicron CMOS does not allow large power supply voltages, 2.5 V is common. This limits the internal signal swing. We can estimate the necessary precision by assuming that
a 3 V full scale range can be achieved for the differential internal signals. This means the LSB is 3 V/4096 or 732 μV. Thus comparator thresholds must be stable and accurate to one half the LSB or 366 μV. Amplifier and sample/hold gains must be stable and accurate to about the same precision, 0.01% (∼ 0.5/4096) of full scale. Charge injection errors in the sample/hold circuits must also be controlled to the same level of precision.

Error Control

There are three types of errors in the digitizer:
1. Offset errors: uncertainties in the comparator thresholds, fixed charge injection from the sample/hold, and amplifier offset.
2. Gain errors: uncertainties in the gain stages and sample/hold gain.
3. Dynamic errors: uncertainties in the timing and amplifier and sample/hold settling times.

Offset and Gain errors will be measured as part of the qualification test on raw chips. These errors do not have to be measured individually. For example the offset error from the comparator, the charge injection offset and amplifier offset will be measured as a single number. These values will be loaded into an on-chip memory. The raw digitized numbers will be used only as indices to tables of “correct values”, which will be used to calculate the true input value. The maximum number of these calibration values is estimated to be 72. With this scheme, we only require stability in the design and process. Based on experience, this level of stability should be achievable over a modest temperature range. In addition these devices can be recalibrated in the field.

Dynamic errors will be controlled by careful design. By means of simulation and prototyping we will design each of the internal functions to have sufficient bandwidth to settle in the required time.

Process

The proposed digitizer requires several amplifiers with a gain of eight. Let us assume that we allow half the bunch period (0.7 ns) to sample and the other half to hold. To settle to 12 bits with a precision of one half the LSB requires nine time constants (e⁻⁹ ∼ 0.5/2¹²) or a rise time of 171 ps (2.2τ with τ = 700 ps/9). To accomplish this the fabrication process must provide a product of gain (8) and bandwidth (1/2πτ) of 16.4 GHz. The IBM process SiGe BiCMOS 6HP/6DM is available through MOSIS and features 40 GHz NPN bipolar transistors along with 0.25 μm CMOS.

Progress Report

The heart of the digitizer is the 3-bit cell as shown in Fig. 2. Most of the components of the circuits have been designed and simulated. These include the comparator, encoder, multiplexer, and op-amp. The performance of the circuits is satisfactory although some improvements in the latter two are still desirable. We concentrate in FY05 on the most critical component of the circuits, sample and hold.
The design of the sample/hold is shown in Fig 3. We use AC coupled stages internally since the waveforms to be digitized have no DC component. This allows for a very simple sample/hold circuit with gain that is set by a capacitor ratio, C1/C2. The DC operating point of the circuit is maintained by a slow feedback loop. The output of the feedback amplifier is driven by MOS transistors biased in the sub-threshold region. This results in very high output impedance.

The switch on resistance is proved to be small enough to allow 9 time constants of charging in 700 ps. A second, half-size dummy sampling switch has been added to cancel the injected charge from the first switch. There is a trade-off between frequency response and distortion which limits the selection of transistor size in the switches. We found two major error sources from the transistor switches — one proportional to the amplitude of the input and one proportional to the slope of the input, which becomes the major error at the highest frequencies. Without any correction we found ourselves limited to between 6 and 8 bits of accuracy. We have settled on a circuit with 2 switches in series which delivers more than the desired precision up to about 1/10 of the desired frequency bandwidth. At higher frequencies we find that we need a correction based on the slope of the input. In simulation we have implemented a differentiator circuit that can correct the value to at least 10 bits of precision at the highest frequencies. We plan to correct the last bit or two in the calibration process described earlier.
We need custom enclosed transistors with guard rings to layout the digitizer to achieve the radiation hardness. On our last chip design project we were able to use component libraries and Cadence rules files developed at LBNL, CERN, and Rutherford, but this is not available for the BiCMOS process we have chosen for this ADC. We have implemented parameterized cells for the transistors (radiation-hard circular gate MOSFET’s) and re-written the Cadence rules files to enable them to be laid out and extracted. We made several practice layouts, including our AC amplifier and a complete sample/hold unit to test the layout and simulation capabilities. We plan to layout the digitizer once we achieved the 12-bit resolution.

Our original plan was to submit in FY05 the layout of the prototype digitizer for fabrication since there are now enough funds accumulated from FY04 and FY05 for the submission. However we encountered significant challenges as we tried to achieve the 12-bit resolution. We decided to spend more time investigating various ideas for improving the resolution rather than rushing to submit the layout. If we submitted a layout with 12-bit resolution based on simulation but achieved 11-bit resolution in the fabricated chip, the chip would satisfy the needs of various BPMs in the ILC. We believe that this is a sensitive strategy given the high cost of fabrication.

Goals for the Year 2005–6

The design and development activities will include:
1. Continued improvement of the 12-bit digitizer
2. Layout and submission of the first prototype 12-bit digitizer
3. Testing of the prototype, including radiation hardness tests

We plan to have one submission in this funding cycle.

Goals for the Year 2006–7

The design and development activities will include:
1. Continued improvement of the 12-bit digitizer
2. Layout, submission and testing of the second prototype 12-bit digitizer
3. Continued system design of the full 12-bit digitizer

We plan to have one submission in this funding cycle.

Budget Description

The design work is performed by an electrical engineer paid for by the Department of Physics of The Ohio State University. He is assisted by a technician paid for by this project. The technician has a Bachelor degree in electronic engineering technology from DeVry University and is currently studying part time for a Bachelor degree in electrical engineering at The Ohio State University. He has worked on the optical electronics for the pixel detector of the ATLAS experiment over the last few years. The travel budget allows the designers to visit SLAC to discuss the design with our SLAC collaborator. The MOSIS cost for the prototype digitizer using the IBM 0.25 Micron SiGe BiCMOS 6HP/6DM process is $54,000. In FY06, we request about half of fund needed to fabricate the second prototype in FY07 with the balance to be requested in FY07.
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* Indirect cost is 49.5% for personnel and travel.
Bibliography

1. Marc Ross, private communication.

2. www.cadence.com