

Project name

Development of a silicon-tungsten test module for an electromagnetic calorimeter

Classification

Detector: calorimetry

Institutions and personnel

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I. Project Overview

The current LD and SiD detector designs call for a silicon-tungsten (Si-W) electromagnetic calorimeter (ECal) as the best option for providing the necessary density and segmentation to implement the *particle flow* method (PF, formerly called *energy flow*) for reconstruction of jets (and taus) at the LC, capable of achieving jet energy resolution of $\approx 0.3/\sqrt{E_{\text{jet}}}$, as recommended by LC physics studies. One of the outstanding technical questions is how to integrate a silicon detector wafer with its readout electronics. Since the number of detector pixels for these ECal designs is on order 50 million, a solution to the integration issue, along with the cost of the silicon detectors themselves, is likely to determine the overall viability of the Si-W approach. A few years ago, we proposed^{1,2} a possible solution to the integration problem and have received LCRD support for two years to pursue this. Our work gives us confidence that we are on the right path and we propose for the next year to complete the initial phase of the R&D – to demonstrate the detector concept with prototypes in an electron test beam – and to move on to the next phase: The development of a full-depth ECal module which incorporates the features required for a realistic LC detector. This module would be part of an international test beam study. The full-depth module requires more funding than is realistically available with the present LCRD program. Hence, its funding is being pursued separately. Here, we focus on completing the development and initial testing of the detector components, the goal being to test a few layers of our prototype detectors and electronics in the lab at Oregon and in an electron beam, hopefully at SLAC.

While we focus on an implementation of our Si-W approach for the SiD design, the basic ideas and R&D are certainly applicable to other Si-W ECal designs, notably LD.

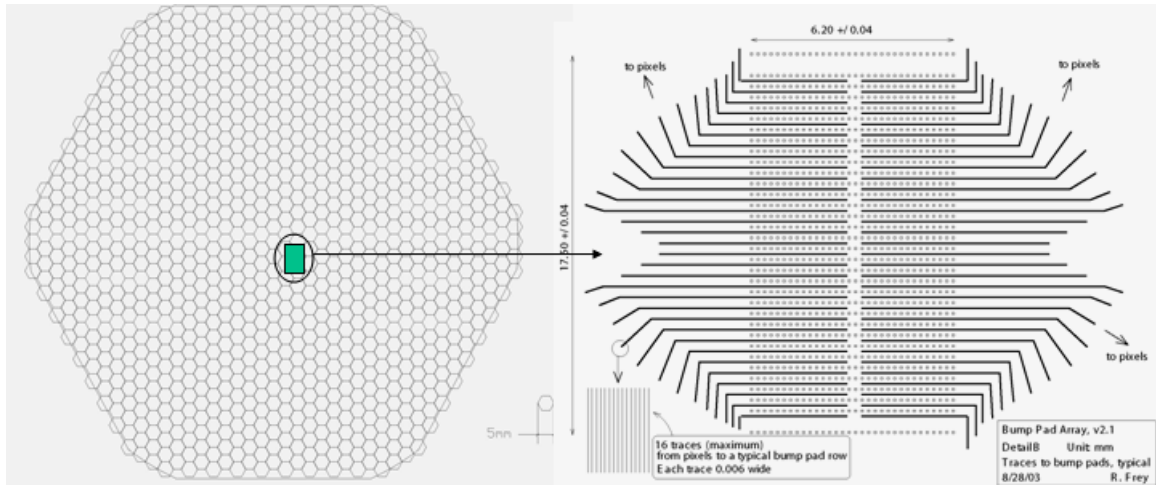


Figure 1. Left: Cartoon of 15 cm Si detector segmented into 5mm pixels. The central rectangle indicates the position and approximate size of the bump-bond array. Right: Schematic of bump bond pad array and bundles of signal traces entering the array from the pixels.

The thrust of our project is to integrate detector pixels on a large, commercially feasible silicon wafer, with the complete readout electronics, including digitization, contained in a single chip which is bump bonded to the wafer. This is shown in Fig.1. The starting point for our design uses a pixel size 5 mm across, based on initial PF requirements for photon-hadron separation. This gives $N \sim 10^3$ pixels per 6-inch wafer. We take advantage of the low beam-crossing duty cycle ($\sim 10^{-3}$) to reduce the heat load using power cycling. This scheme has several important properties:

1. The channel count is effectively reduced by a factor N .
2. The cost, to first order, will be independent of the ECal transverse segmentation.
3. Readout gaps can be small (~ 1 mm), thus maintaining the small Moliere radius intrinsic to tungsten.

The first property, we feel, is necessary for any realistic highly-segmented ECal. In this case, the electronics is likely to be a relatively small fraction of the ECal cost. The second point makes the design flexible, so that one can optimize to meet the physics goals. The third is an optimization of the physics capability of the ECal at a given (barrel) radius. For example, the angle subtended by the Moliere radius for an ECal at radius 1.25m with our design is smaller than one with 3mm readout gaps at 1.7m. Hence, this has a significant impact on both performance and overall detector cost.

We note that for a Si-W ECal, the features above remain unique to this R&D.

Collaborations. First, within this R&D, the collaboration consists of the Oregon and SLAC personnel listed above, in addition to V. Radeka of BNL who has collaborated with us extensively on the electronics design. Our R&D collaboration has been holding weekly meetings by telephone for over two years. Between Oregon and SLAC the activities roughly break down as follows:

1. Silicon detector design, procurement, characterization, and testing (Oregon)
2. Readout chip design, procurement, and testing (SLAC)

Recently, we have begun discussions with the HEP group at UC Davis in connection with their bump-bonding facility. This appears to be a good possibility, and members of the UC Davis group will presumably join our R&D effort. In addition to the hardware work, Oregon plans to continue related simulation and software activities. These include, but are not limited to, EGS4 and Geant4 studies, comparisons between the two, and development of PF algorithms. Ultimately, we will use robust PF results to optimize the calorimeter. The LC community is still a long way from this point, although the recent focus on a few detector designs is helpful.

Within the ALCPG, Oregon has strong ties to the Calorimeter Working Group³, both in management and involvement in studies. We report regularly to this group, as well as at the ALCPG workshops.

We also have good interactions with the proponents of the Si-W ECal of the CALICE R&D consortium. We note that the goals of the two efforts are considerably different. While we are pursuing R&D to develop detectors and electronics which we feel will closely resemble the final ECal, the CALICE effort has focused more on gaining experience with detector fabrication and in developing a working test beam module. Since both of these approaches are important, it is premature, and probably counter-productive to merge efforts at this stage. In the meantime, we share our thoughts and concerns. The level of collaboration will increase as we approach full-module test beam studies. In fact, both groups are part of a joint MOU for a potential test beam at FNAL.

This document follows with a short progress report of the recent R&D, a summary of the proposed work, followed by the budget and budget explanation. Most of the details not presented here are collected at <http://www.slac.stanford.edu/xorg/lcd/SiW/> or in the cited references.

II. Progress Report and Status

Electronics

Significant progress has been made on the readout chip (ROC) design. A block diagram of the current design for a LC with cold technology is given in Fig. 2 and indicates the main functional elements of the design. A reset is issued in 100ns if no signal above threshold (≈ 0.3 MIP) is detected. (The interval between beam crossings is 337 ns in the TESLA cold design.) Signals above threshold are integrated for a longer time and the signal charge is stored on capacitors until the end of the bunch train (2820 beam crossings). The depth of the signal storage is currently set at four, which appears to be easily sufficient for the expected background rates per pixel in the ECal barrel (although this may not be sufficient in the low-angle endcap region). The area required per readout channel is an important parameter in our design, with an important contributor being the 10 pf feedback (and calibration) capacitors on the input stage required to accommodate a maximum expected signal of ≈ 2500 MIPs at shower maximum (at about $10 X_0$ depth) for 500 GeV electrons⁴. The dynamic range and MIP resolution are both accommodated using two ranges, each of 12-bits. The range is selected dynamically by switching in the

appropriate feedback capacitor on the first stage amplifier, a novel feature of this design. In 0.25 micron technology, the current design uses about 0.03 mm^2 per channel, which is easily accommodated in our layout for a 1024 channel ROC. Another important design constraint is power consumption (heat). Most of the ROC power goes to the analog front end, for which the power can be turned off between bunch trains. The duty cycle is roughly $1/200$, which is sufficient to reduce the average power of the entire 1024-channel ROC to about 20 mW. This is roughly a factor of two below our estimates for the heat load which would require active cooling. Hence, we plan to carry the heat load to the edges of the ECal modules passively, via the tungsten radiators.

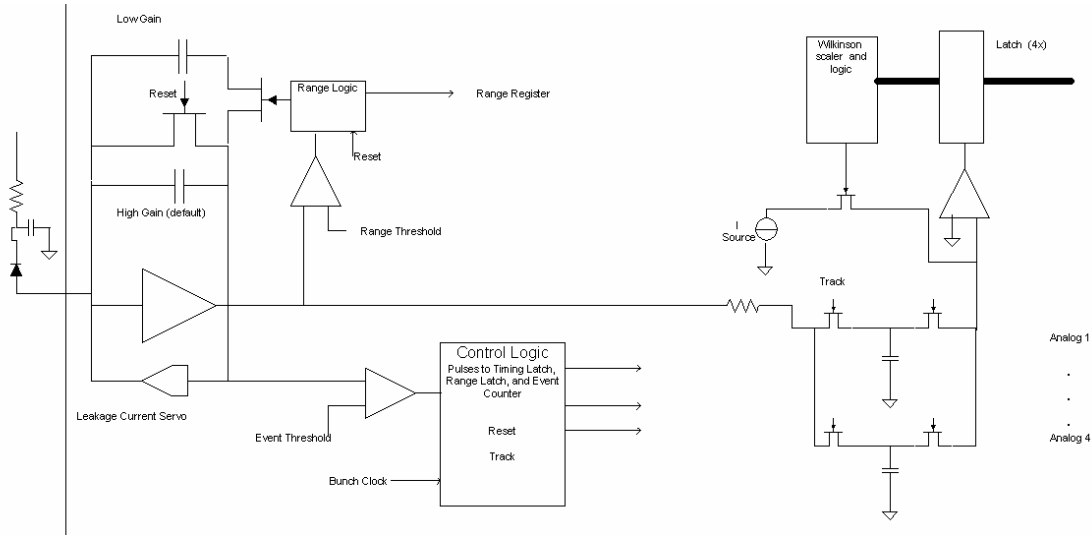


Figure 2. Schematic of one channel of the ROC optimized for the cold LC.

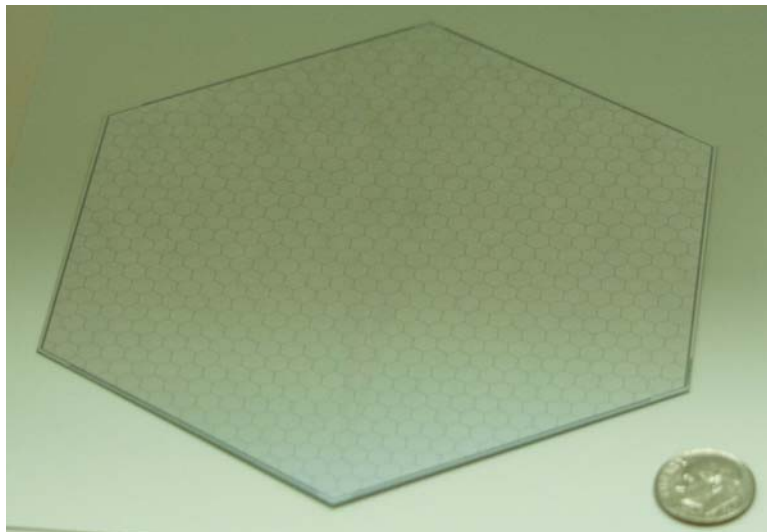


Figure 3. Prototype silicon detector in the lab at Oregon.

Silicon Detectors

In Fall 2003 we ordered a set of 10 silicon detectors from Hamamatsu Corp. using a combination of LCRD and SLAC funding. The order was based on a specification document⁵ which we developed for potential vendors. A separate document⁶ discusses the various tradeoffs necessary to minimize detector noise and inter-channel crosstalk, retaining an excellent SNR for MIPs of ≈ 20 . The order was received at Oregon in January

2004. An image of one of the detectors is shown in Fig. 3. These detectors in principle meet the requirements for a full Si-W ECal. The hexagonal pixels, 5mm across at maximum, are clearly visible. The bump-bond array and signal traces, being below the passivation layer, are not easily visible in this image.

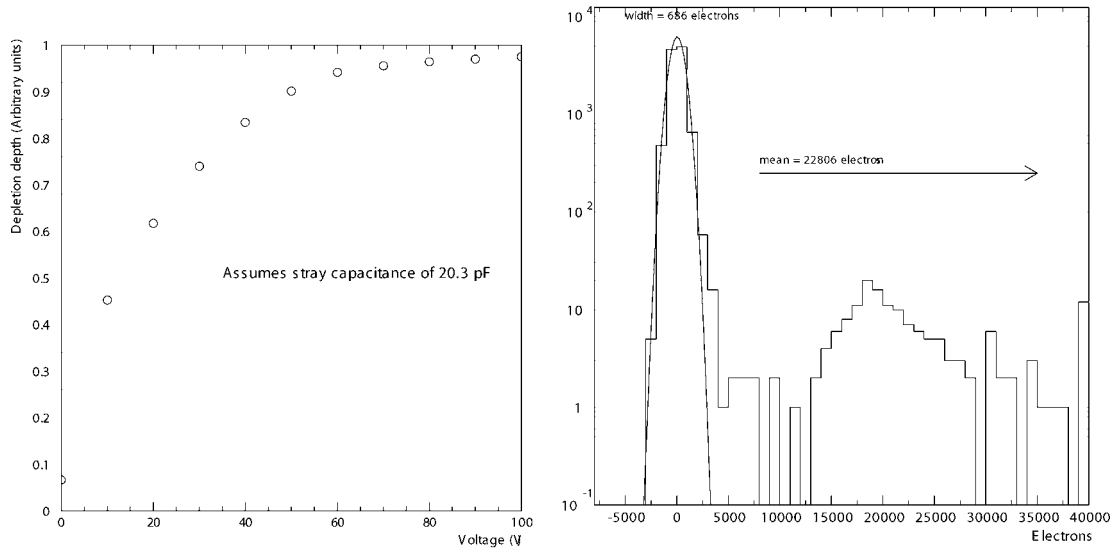


Figure 4. Left: A typical depletion curve for a prototype pixel. Right: Measured signal charge distribution for cosmic ray data.

We have performed a number of standard measurements of the detectors in our lab at Oregon, such as capacitance, depletion voltage, and leakage current. A typical depletion curve is shown in Fig. 4. Such characteristics are entirely as expected.⁷ The right-hand panel of Fig. 4 shows a single-pixel signal charge distribution for cosmic ray data. The pixel was connected to a channel of commercial electronics which has electrical characteristics very similar to those of the prototype ROC design. The charge scale was independently calibrated. The MIP peak near 2.0×10^4 electrons, consistent with expectations for a fully-depleted 300 μm thick detector, is clearly visible. Cosmic-ray triggers for which the muon missed the target pixel enter the distribution as noise, and we see that this is as expected, with a rms of ≈ 1000 electrons.

A significant effort this past year went into the understanding of issues associated with timing measurement in a Si-W ECal. This became a significant issue in the run-up to the LC technology decision by the ITRP. In the warm LC, pileup of 2-photon generated backgrounds can pose a significant problem if the detector does not have timing resolution comparable to the 1.4ns beam crossing interval. A good timing measurement with a Si-W ECal could be crucial. Despite initial skepticism from some, we were able to demonstrate^{7,8} both in calculation and in measurement in our lab that single-pixel resolutions of ≈ 5 ns are feasible, providing ≈ 1 ns resolution for a 30-hit MIP track, and thereby in principle limiting pileup to about 3 beam crossings.

Tungsten

As reported last year, we found an excellent vendor for tungsten. Using LCRD funds, we purchased enough 2.5 mm and 5.0 mm thick plates of sufficient size for a full-depth test beam module. These are at Oregon. Their measured characteristics are fine.

Evaluation of Progress

We have made good progress during the last year. We have excellent prototype detectors, and despite the need to move from electronics compatible with warm LC technology to cold technology, the prototype ROC design is rapidly converging. The expectation is that the design will be submitted for fabrication of prototype chips in late Spring 2005.

III. Proposed Research

As stated above, SLAC is developing the first readout chip prototypes for a cold LC. It will be implemented in 0.25 μm technology. These prototypes will have two rows (out of 32), each having 32 channels, or 64 total. This will save a considerable amount of money, while allowing functional evaluation. We are currently reviewing various options for configuring these chips with the Hamamatsu prototype detectors. One option is to bump bond a few of these chips to the 32 \times 32 bump pad array on the detectors, providing readout of a contiguous swath of pixels. This will permit initial lab tests, but will also make a "technical" test beam run with a few such detectors a feasible possibility.

To pursue the possibility of such a beam test, we have sent to SLAC a proposal to run in the End Station A line. A broad range of electron energies can be delivered at very low, to moderate rates. However, the SLAC beam schedule is highly uncertain at this time.

We have made progress with the design of the gap between layers of tungsten. As discussed above, this directly affects performance, so we must minimize the gap, but at the same time produce a robust structure. This design must also integrate the PC board used to provide power to the readout chips, any external capacitors needed for the power, and the traces used for control signals and readout of the chip. Our goal, which does not appear to be impossible, is to achieve a 1mm gap.

As part of the technical test beam preparation, we will need to design and procure the PC motherboard for the gaps. We will attempt to make these initial boards consistent with the boards eventually required for the 1mm gaps. We are requesting LCRD funding for this.

The technical beam test will require a back-end readout of the ROCs. A "data concentrator" board (eventually an integrated in-detector chip) will be needed for the full test module, followed by standard VME or equivalent. However, for the initial beam test we believe we can use a commercial FPGA card which would plug in directly to the PCI slot of a computer. We can also use this in our lab measurements of cosmic ray or IR laser response. This card is relatively inexpensive (2k\$) and is included in our request.

We intend to pursue a number of improvements which would be included in the design of a second round of prototype detectors, presumably those which would be used for the full-depth test beam module. These improvements fall into two general categories: small modifications to detectors which otherwise closely resemble our current prototypes, and more substantial departures from the prototypes. The former type includes further optimization of the width and thickness of signal traces on the detector to optimize SNR.

For example, the pixels which lie beneath the bump-bond array have an especially large parasitic capacitance which could be reduced with layout optimizations. The dimension of the bump array itself may likely need to be reduced to reflect the (new) smaller electronics channel footprint. The next detectors will need small cutouts on one corner to allow for a mechanical standoff. And there will need to be a good method for applying the silicon bias voltage to the detector backsides.

The main example of where a bigger departure may be considered is with the desire to increase the thickness of the insulation layer between pixels and the metallized signal traces, thus reducing the capacitance and improving SNR. Our prototypes use SiO₂ insulation, and this can not be easily thickened without increasing the entire detector thickness. (Thicker detectors actually provide signals which are too large, since they then require a larger front end feedback capacitor, hence a bigger footprint.) Alternatives to SiO₂ are possible commercially, and understanding these possibilities may be useful at some stage. However, this more closely resembles a generic R&D project, and we don't intend to request funding from LCRD at this time.

Preparing a few prototype layers for the technical test beam discussed above will bring to a close what we might call the first phase of our R&D. The next important goal is to prepare the full-depth module for the international test beam effort. As mentioned above, we would incorporate our findings from phase one into the detectors and ROCs for this module. These would be full 1024 channel ROCs, so will require full secondary readout, attention to the cooling, a real mechanical structure, and so forth. The goal of the full beam test is important to the overall LC detector R&D: We need to be able to describe hadronic showers at the level of detail which the LC calorimeters, with their fine segmentation, will provide. Once we have validated a simulation code in the test beam, we can confidently design and optimize our detectors for jet physics at the LC. The ECal is essential for this, since approximately half of hadrons begin to shower in the ECal. And we feel that the fine segmentation of our design will provide a very detailed view of the showers. Since the full-depth module will require funding beyond the current scope of LCRD, we are seeking funding from the NSF MRI program for the bulk of the required support.

IV. Budget Explanation

We note that within our R&D collaboration, only Oregon requests LCRD funding. We include any applicable overhead in our budget numbers given below. At UO, this applies to equipment only if the cost is less than 5k\$.

For the "technical" beam test we request 5k\$ for the design and fabrication of mechanical fixtures.

The lab test equipment request includes the following: Low and high voltage power supplies (4k\$), a probe card and associated fixtures (8k\$), test amplifiers (2k\$), and clean room supplies (2k\$). The FPGA card (2k\$) mentioned above for the back-end readout is included here.

For the development of our printed circuit motherboard for the beam test we request 4k\$ for its design, 4k\$ for its fabrication, and 2k\$ for the required wire bonding to the ROC.

We currently employ an equivalent of two undergraduate physics students in our R&D at the level of 10 hours per week. We request support for 50 weeks per year of support for each of two students, making about 10k\$.

The budgets beyond the first year are completely uncertain at this time, since the direction of the R&D depends crucially on the outcome of other funding requests to support the development of the full-depth prototype, and the SLAC budget and beams schedule.

V. Budget

Year 1

Institution	Item	Cost
Oregon	Mechanical design and fixtures for test beam	\$ 5,000
Oregon	Probe and custom test equipment for lab	\$18,000
Oregon	Design and fab. of PC board	\$10,000
Oregon	Two undergraduate students, at 500 hours each	\$10,000
Oregon	Travel and shipping (for test beam)	\$ 2,000
Oregon	Oregon total	\$45,000
SLAC	SLAC total	\$0

References

1. M. Breidenbach, talk at Chicago LC Workshop, Jan. 2002, <http://LCworkshop.uchicago.edu/>; updated at Cornell workshop, July 2003, <http://www.lns.cornell.edu/LC/workshop/>.
2. R. Frey, talk and proceedings paper from Calorimeter 2002, Pasadena, CA, March 2002, documents available at <http://3w.hep.caltech.edu/calor02/> ; talk presented at Linear Collider Workshop, LCWS2002, Korea, Aug. 28, 2002, <http://lcws2002.korea.ac.kr/>.
3. ALCPG Calorimeter Working Group web page: <http://www.slac.stanford.edu/xorg/lcd/calorimeter/>
4. R. Frey, Silicon session talk and Proc. Paper, Calorimeter 2002, see Ref 2.
5. R. Frey and D. Strom, Silicon Detector Specifications, July 2003, http://www.slac.stanford.edu/xorg/lcd/SiW/documents/SiSpec_v3.pdf .
6. D. Strom, Silicon Detector Properties, Sept. 2003, http://www.slac.stanford.edu/xorg/lcd/SiW/documents/strom_specs_Sep03.pdf .
7. D. Strom, talk presented at IEEE NSS Conf., Rome, 2004.
8. D. Strom, talks at Calorimeter 2004, Perugia, and Victoria ALCPG LCWS, July 2004.
9. See links DF at <http://www.slac.stanford.edu/xorg/lcd/SiW/SiW.html> .

(Some talks also available at the web site of the American Linear Collider Calorimeter Group: <http://www.slac.stanford.edu/xorg/lcd/calorimeter/>)

Relevant experience of proponents

The SLAC group has vast experience in design of e^+e^- detectors, including design and implementation of the readout electronics for most major detector systems for the SLD detector and several BaBar sub-systems. Of specific relevance, the group led the design and fabrication of the electronics for the silicon strip detectors for the GLAST experiment. Graf is co-leader of the American Linear Collider Physics Group (ALCPG) simulations group and is the leader of the SLAC LC simulation group.

Strom and Frey have each worked on silicon-tungsten luminosity calorimeters for OPAL (Strom) and SLD (Frey). Strom in particular was a key person in the OPAL silicon-tungsten development. Frey is co-leader of the ALCPG and SiD calorimeter working groups. Strom is co-leader of the test beam coordination sub-group of the ALCPG working group. They have extensive experience using simulation codes such as EGS4 and GEANT to analyze and characterize detectors.