

Development of thin silicon sensors for tracking

Classification (subsystem) Tracker.

Personnel and Institution(s) requesting funding

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Project Overview

One of the possible detector options for the LC is SiD which incorporates a Silicon/Tungsten calorimeter with a precise silicon tracker and vertex detector. The tracker design includes a compact silicon tracker with 5 layers in the central region and five disks per end. The tracker is expected to provide excellent momentum resolution and pattern recognition in a compact volume and therefore minimizes the cost of the calorimeter. Now that the LC technology has been selected it is important to develop the SiD detector concept into a detailed detector technical design report. In order to achieve this goal there are critical questions that have to be addressed. These questions have been summarized in a document by Breidenbach, Brau, Jaros and Weerts[1]. This proposal will address the issue of material minimization and pattern recognition in the endcap outlined in [1].

Material Minimization

The objectives of LC physics include the precision studies of the Higgs and new physics which can only be achieved by a detector with:

- excellent flavor tagging efficiency and purity for bottom and charm quarks
- superb momentum resolution with polar angle coverage down to about 110 mrad.
- two jet mass resolution comparable to the natural width of the W and Z bosons
- hermeticity to achieve a precision measurement of the missing momentum

These requirements lead to a fully integrated detector and the implementation of particle flow algorithms to measure the jet energies.

Therefore it is important that the LC tracking and vertexing systems achieve excellent momentum resolution even in the forward region and for low momentum tracks, good pattern recognition, and extremely precise impact parameter resolution to distinguish secondary and tertiary vertices for flavor tagging. R&D is necessary to substantially improve the vertexing and tracking subdetector performance that was achieved for LEP/SLC to cope with increased jet multiplicity, higher track density in more collimated jets and larger backgrounds[2].

Material minimization is important both to achieve excellent impact parameter resolution and for the precise measurement of low momentum tracks. Therefore it impacts both silicon

pixels that provide precise space points near the interaction region and a silicon microstrip tracker further from the primary interaction region, and the measurement of tracks at small angle in the forward region.

Preliminary simulations have been performed comparing the momentum resolution achieved by the silicon tracker in a SD Thin and SD Thick scenario in the barrel. The results indicate that the SD thin tracker with 3 inner layers of sensors 200 μm thick and 2 outer layer of standard thickness silicon (300 μm) could achieve similar or better momentum resolution than a TPC tracker[3].

Several questions must be answered in order to understand if this option is truly feasible:

- Can thin detectors be manufactured with a reasonable yield?
- What signal to noise ratio and resolution can be obtained with thin sensors?
- Can mechanical handling and mechanical support challenges be met?

The R&D program at Purdue University will answer these questions in a very cost effective and timely way.

Current Status of Research on Thin Silicon Sensors at Purdue

Using DOE ADR funding, the Purdue group explored in 2002 the capabilities of several vendors to produce thin silicon sensors and received quotes from two vendors, SINTEF and MICRON. Both vendors were extremely interested in developing this new product line. After reviewing vendor capabilities we selected MICRON as the vendor in 2003.

MICRON delivered in December 2003 thin silicon strip sensors in the following thicknesses: 150, 200, and 300 μm in 4 inch technology. The sensors were manufactured using the masks developed for the silicon layer mounted on the CDF beam pipe. Each sensor is 7.84 cm long, 0.843 cm wide, with 256 channels designed to be connected to 128 readout channels. A photo of the corner of a sensor is shown in fig. 1.

We also received double sided silicon pixel sensors on 6 inch wafers in spring 2004. These wafers are 200 and 300 μm micron thick. Each n^+ pixel has a dimension of 100 $\mu\text{m} \times 150 \mu\text{m}$ matching the PSI46 0.25 μm chip developed for the CMS pixel detector at the LHC.

We have performed an electrical characterization of the thin microstrip sensors. This includes measurement of the bias voltage, leakage current (I_{leak}), interstrip capacitance (C_{IS}), the coupling capacitance (C_C), the interstrip resistance (R_{IS}) and bias resistance (R_{bias}). The measurements were performed on a strip by strip basis to determine the overall sensor quality.

The electrical performance of the thin silicon strips is summarized in Table 1. The depletion voltage of the sensors has been found to scale with the thickness as expected. The 300 μm thick sensors have a depletion voltage of about 85 V. The depletion voltage decreases to 30 and 15 V for 200 μm and 150 μm sensors respectively.

As an example we show the leakage current of the 200 μm sensors in fig. 2. All seven 150 μm thick sensors pass all the specification we had set including having a leakage current below $< 50 \text{ nA/cm}^2$ at a bias voltage equal to twice the depletion voltage. The low leakage current of the sensors we have received confirms that thin detector processing can be successfully achieved. The measurements of the capacitance and resistance indicates that the resolution performance should not be compromised by reducing the sensor's thickness.

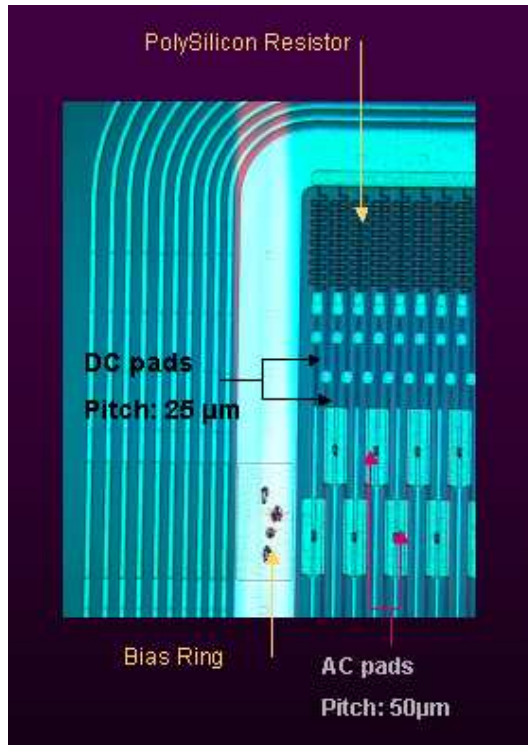


Figure 1: Corner of a thin silicon microstrip sensors. The photo shows the guard ring, the biasing scheme, the strips and the bond pads.

In summary, the results already at hand are extremely promising and indicate that further studies with a readout chip are the next logical step. Measurements of the pixels sensors have still to be conducted.

Future R&D for thin silicon sensors

A critical step to fully evaluate the feasibility of thin sensors for the LC is to determine the Signal to Noise ratio (S/N) and the charge collection efficiency. In a silicon detector, the signal for a charged particle depends on the path length the particle traverses in the silicon and so S is inversely proportional to the thickness. With currently available electronics the noise is expected to be low enough that reducing the silicon thickness from $300\ \mu\text{m}$ to $200\ \mu\text{m}$ would still allow a S/N above 15. For example, the SVX4 chip has a noise of 900 electrons for a capacitive load of 20 pF while the most probable signal for a $200\ \mu\text{m}$ sensor is 14,440 electrons, yielding a S/N of 16. However, in a thin silicon sensors there is also an increased capacitive coupling between the two sides of the sensor, which might increase the noise. Maintaining an acceptable S/N is critical for the long ladder design proposed for SiD[3]. The charge collection efficiency, which also is sensitive to the capacitive coupling to the backplane, has also not been measured for thin silicon sensors.

To study these effects we will use in the first instance, the laser test stand already in place at Purdue to conduct studies with the SVX4 chip developed for Run 2b of the Tevatron. This chip is not optimized for LC applications but is suitable to compare the performance of sensors of different thickness.

Table 1: Comparison of DC characteristics of 300, 200 and 150 μm thick sensors measured at Purdue University. We follow the same notation used in the text with leakage current (I_{leak}), interstrip capacitance (C_{IS}), the coupling capacitance (C_C), the interstrip resistance (R_{IS}) and bias resistance (R_{bias}). We define two different grades to the sensors according to their I_{leak} . Grade A (B) sensors have a I_{Leak} at $2 \times V_{dep} < 50 \text{ nA/cm}^2$ (4000 nA/cm^2)

	I_{leak}	C_C pF/cm	C_{IS} pF/cm	R_{IS} G Ω	R_{bias} M Ω
Specs	Grade	> 10	<1.2	> 1	1.5 ± 0.5 < 10 % variation
300 μm	3 Grade A 2 grade B	> 15	< 0.9	> 1	0.5 ± 0.2 < 5 % variation
200 μm	3 Grade A 2 Grade B	> 20	< 0.9	> 10	1.8 ± 0.10 < 10 % variation
150 μm	7 Grade A 0 Grade B	>15	< 0.9 pF/cm	> 10	1.8 ± 0.10 < 10 % variation

Ultimate functionality and performance characteristics will be established in a test beam. We plan to take advantage of the MT4 test beam facility at Fermilab and to measure the charge collection efficiency, position resolution, and signal to noise ratio in the beam.

The mechanical aspect of thin silicon are frequently overlooked but they are equally challenging and will require a similar amount of time to develop. There are three issues:

1. Acceptable yield
2. Handling post manufacture at HEP labs
3. Mechanical support

We address (2) and (3) here, the vendor is responsible for (1). We will produce thin silicon sensors which will be wire-bonded to existing electronics. These structures will be used with prototype mounting schemes. Full Finite Element Analysis models both mechanical and thermal will be developed. CTE mismatches are more serious for thin silicon sensors and so one example of the studies that will be performed is temperature cycling of the silicon, electronics and the mounting assembly. The mechanical studies will have an impact not only for microstrip sensors but also for CCDs, MAPS (Monolithic Active Pixels Sensors) and HAPS (Hybrid Active Pixels).

Finally, in parallel and in conjunction with other groups in the US, Asia and Europe we will study with Monte Carlo how to optimize the tracker design.

Unique Facilities at Purdue

The proposed effort builds upon our experience in design and testing of silicon micro-strip and silicon pixels for CDF and CMS. We have access to CADENCE design tools and DESSIS simulation tools. The mechanical aspects of the project build upon our experience in the mechanical design, fabrication, and assembly of the silicon detector for CLEO III, and the mechanical design and prototyping of parts of the CMS forward pixel detector.

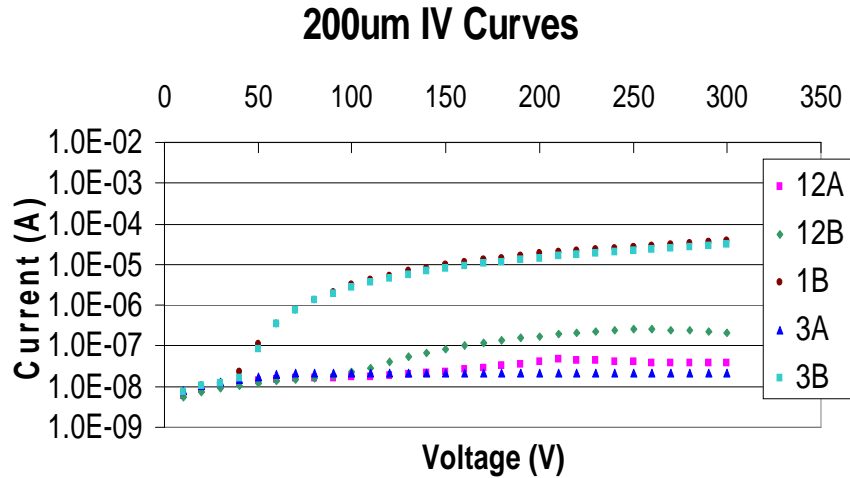


Figure 2: IV measurement for 200 μm thick sensors.

The detector facility at Purdue University contains two fully equipped clean rooms for the design, testing and assembly of detectors for High Energy Physics. These clean rooms are part of a complex dedicated to microstructure detector development and fabrication including silicon strip and pixel devices and micro pattern gas detectors. The total clean room space is 3000 sq ft in three laboratories containing a CMM, wirebonder, electrical testing equipment, probe stations, optical tables, microscopes and high precision measuring devices. The labs are fully equipped with computer facilities for control, data acquisition and analysis. The labs have both temperature and humidity control and HEPA filtering of the airflow. Included in the clean rooms is additional space of class 1000. In a separate location there is a detector irradiation facility with an X-ray source and an ultra clean gas delivery system.

Other technical resources are also available, such as machine and electronic shops within the physics department, a central machine shop and state of the art facilities on campus, such as SEM, TEM (Transmission Electron Microscopy) and EDS (Energy Dispersive Spectroscopy). In addition to the technical staff, an engineer and technician, there is the normal complement of graduate students and research associates working on specific projects. There is also an exceptional pool of talented undergraduates who work on R&D and detector construction projects.

Results from Prior Research

Our group has not received previous funding for LC projects. We are been involved with the LC activities by starting the thin silicon studies using ADR funding, attending LC workshops and communicating with the SiD effort. The Purdue group has considerable expertise in the development of silicon detectors. We played an important role in the design, installation and commissioning of the silicon vertex detector for CDF. The CLEO III silicon detector was built at Purdue. We are now playing a strong role for the CMS forward pixel project.

FY2005 Project Activities and Deliverables

The first year activities will focus on the studies of the thin sensors 300, 200 and 150 μm thick with the SVX4 chip. This will require a PCI based data acquisition system. This system was developed for Run 2b. New boards have to be designed to readout the sensors mounted with the chip. The measurements will be performed by a graduate student under the supervision of Petra Merkel who is already very experienced with this system.

We are also planning to participate in the simulation activities that are gaining momentum in SiD.

The deliverables in the first year will be a quantification of the importance of material minimization, based on more sophisticated MC studies, and an experimental measurement of the performance of thin sensors.

FY2006 Project Activities and Deliverables

In the second year we expect to start studies of the mechanical mounting and the stability of thin silicon strips. There are several ladder designs that are under discussion with the SiD community. One achieves material minimization through a long ladder. The other relies on a short ladder design based on carbon fiber - rohacell support.

1. Studies of alignment and fabrication of low mass support frames will be conducted at Purdue. Metrology of thin silicon samples will be performed during cooling cycles. These will need to be conducted at cryogenic temperatures for CCD applications.
2. Finite Element Analysis (FEA) will be performed to understand the mechanical stability of thin silicon sensors and mechanical support structures.

The second year deliverable will be a systematic study of the mechanical issues associated with thin silicon strips.

FY2007 Project Activities and Deliverables

In the third year we will continue the simulation effort and the mechanical studies. Systematic studies will be performed with the strips to determine the resolution and charge collection efficiency in a beam tests. Hopefully by that point an optimized LC readout chip might be available and a more realistic bench mark of thin silicon strip sensors will be performed.

The main third year deliverables will be a first evaluation of the potential gain in resolution that can be achieved with thin, silicon sensors. We expect to perform:

- Beam tests for structures wire-bonded to electronics.
- Simulation of charge collection properties of structures, with both two-dimensional and three-dimensional simulation packages, CCE, pulse shape, operating conditions etc.

Budget justification: Institution 1

We request funds to support 50% of a graduate student and a 50% of a postdoc. The remainder of the support for the student will come from the Purdue CDF group. The graduate student is charged at the rate set by Purdue University for 2005/2006, increased by an estimated 5% per year thereafter. The remainder of the support of the postdoc will come from the Purdue CDF and CLEO groups. The postdoc and the graduate student will carry out the simulation studies and will evaluate the thin silicon sensors under the guidance of the senior personnel.

We request travel support for three trips each year to institutions working on LC vertexing. We are also asking for equipment items.

First Year Budget

During the first year we request \$ 10.45 K to set up a PCI DAQ system at Purdue. This includes:

1. **A dedicated PC: \$2500**
2. **PTA board** a PCI test adapter board based on the Altera FPGA Chip to interface between the PC and the PMC card: **\$ 1150**
3. **PMC a programmable mezzanine card** based on Xilinx FPGA Chip to readout the ROC: **\$1150**
4. **2 power supplies: \$ 1400**
5. **50 SVX4 and sensors carriers boards: \$4,250**

Second Year Budget

The second year equipment budget will allow Purdue to build a system to study the mechanical issues connected with the thinning of sensors and readout chips. The study will include precision measurement of the stability of the support schemes including temperature cycles. Some of these studies will be conducted with blank silicon and some with functional sensors built using ADR funds. The graduate student at Purdue will work closely with the Purdue mechanical engineer (Kirk Arndt) to perform the temperature cycling studies. Thin sensors provided by ADR funding will allow a determination of the yield and the minimum thickness that is achievable by the vendors.

Equipment breakdown:

1. **Precision alignment tooling: \$1.5K**
Vacuum holders for sensor/ROC assemblies and holder for support frame that precisely aligns the modules to the support frames. Cost is based on recent experience with similar tooling for CMS pixel R&D efforts.
2. **Fabrication and assembly of a low-mass support frame: \$2.2K**
Support frame will be either beryllium or carbon composite and will need to be of reasonably high precision.
3. **Thinned silicon, 2 batches @ \$1K per batch: \$2K (at no cost - ADR funding)** Cost estimate is based on previous purchases.
4. **Metrology: \$2.0K** This involves modifications to allow us to mount our samples in a dry chamber which can be cycled to a low temperature. The modifications require an optical window to allow inspection and metrology during the temperature cycling. This will be similar to a chamber built by BTeV for their pixel studies but modified to allow for operation at cryogenic temperature for CCDs studies.

Third Year Budget

The third year budget requests equipment to setup the beam test at Fermilab. This will include a duplication of the PCI based DAQ and the mechanical assembly of a dedicated telescope.

Three-year budget, in then-year dollars

Three-year budget, in then-year K\$

Institution: Purdue University

Item	FY2005	FY2006	FY2007	Total
Post Doc (0.5 FTE)	22.0	23.1	24.3	69.4
Graduate Students (0.5 FTE)	9.8	10.3	10.8	30.9
Graduate Fee Remissions	2.62	2.75	2.89	8.26
Graduate Student Insurance	.45	.47	.5	1.42
Scientific Equipment	10.45	5.7	10.0	26.15
Travel	2.5	2.5	2.5	7.5
Indirect costs	17.47	18.30	19.19	54.96
Employee Benefits (Post doc)	9.02	9.47	9.96	28.45
Employee Benefits (Graduate)	0.039	0.041	0.043	0.12
Total direct and indirect costs	74.35	72.63	80.18	227.17

References

- [1] M. Breidenbach, H. Weerts, J. Brau, and J. Jaros
<http://www-sid.slac.stanford.edu/Documents/CriticalSiDQuestions.pdf>
- [2] Tesla, TDR, <http://tesla.desy.de/newpages/TDRCD/start.html>
- [3] The long shaping ladder option is described in Bruce Schumm's talk at the Victoria meeting. The short ladder option is described by Tim Nelson's talk at several SiD meetings.