TPC VLSI Readout R&D

Tracking

Personnel and Institution(s) requesting funding

M. Battaglia, University of California at Berkeley and Lawrence Berkeley National Laboratory

G. Abrams, J. Kadyk, M. Ronan and W. Wenzel, Lawrence Berkeley National Laboratory

M. Chertok, M. Tripathi, R. Erbacher, University of California at Davis

Collaborators

K. Einsweiler, Lawrence Berkeley National Laboratory

Project Leaders

Marco Battaglia
MBattaglia@lbl.gov
(510) 486-7029

and

Maxwell Chertok
chertok@physics.ucdavis.edu
(530) 754-7351

Project Overview

The proposed R&D program aims at a proof of concept and the development of a novel read-out technique for a Time Projection Chamber (TPC) tracker, based on highly integrated VLSI electronics, adapted from hybrid Si pixel detectors.

Significant R&D activity on a TPC based on Micro-Pattern Gaseous Detectors (MPGDs) is presently being carried out worldwide to develop a large volume tracking chamber with three-dimensional particle track reconstruction, matching the challenging requirements of the ILC physics program. Not only will the momentum resolution at the ILC need to improve by almost an order of magnitude compared to the performances of detectors at LEP and SLC, small readout cells and large channel multiplicity will have to be addressed. The Main Tracker device must also be light, so as not to degrade the calorimetric measurements of neutral electromagnetic particles and hadrons, thus restricting the amount of electronics which can be installed at the chamber end-plates. The concept of a large detector based on a 3D central tracker, providing continuous reconstruction of charged particle tracks, has been receiving significant support in the physicists community promoting the ILC studies. Designing a TPC, able to provide the required momentum resolution with thin, highly integrated endplates is a centerpiece of this concept.

Similar challenges have already been met, and solved, in the development of high resolution vertex detectors. The R&D, initiated at LEP and SSC and continued in applications at experiments at the LHC and BTeV at the Tevatron, has developed into a new paradigm for applying high-volume commercial CMOS processes to readout electronics for tracking in high energy physics. This approach allows very complex system-on-chip developments through VLSI technology.

We propose to use a VLSI chip, developed for the readout of the charge carriers generated in a Si $p-n$ junction, to detect and digitize the charge generated in the sensitive volume of a TPC and amplified through a MPGD layer.

A European collaboration has very recently demonstrated this principle, obtaining 2D images of ionizing particles with the MediPix chip, developed for medical imaging, in a drift chamber (see below). This proposal intends to follow-up on the path of work started by that group, build-up expertise on this highly promising technique in the US and expand it into a pioneering study of TPC performance and integrated 3D custom device design.

For the proof of concept of full 3D imaging, we propose to use the ATLAS pixel FE-I3 chip, developed at LBNL and adopted for the ATLAS pixel detector at the LHC. The chip active size is 7 mm$\times$11 mm. The chip contains 2880 channels of charge sensitive amplifiers and fast digital readout operating at a 40 MHz clock. The pixel dimension is 50 μm high and 400 μm wide. The high gain preamplifier is optimized for the typical signal of Si detectors, corresponding to $\simeq$ 20k e^- equivalent. Each time an individual discriminator fires, the pixel address, time and charge information of the hit are generated. The charge is determined by the time-over-threshold. The time is obtained in increments each 25 ns for the 40 MHz cycle. Hits are stored on-chip until an external trigger prompts the readout. The FE-I3 chip is equipped with input pads in the form of 20 μm metal octagons with a 12 μm opening in the insulating passivation layer. In order to avoid discharges in the high field between the MPGD and the chip, the insulating material needs to be reduced by a post-processing in which a thin conductive layer is deposited and the input pads are extended to cover the majority of the anode plane. The proposed test will allow real 3D imaging of the ionization tracks in a small volume TPC.

Broader Impact

Detector development projects provide a very important component of a well rounded graduate student training. The educational impact reaches far beyond the academic world because a large fraction of the students find employment in industry. The activity described in the present proposal will be carried out as a collaboration between two Universities (UC at Berkeley and Davis) and a National Lab (LBNL). We plan to involve both graduate and undergraduate students in the activities. A group of undergraduate students is already working at LBNL on ILC physics questions within the framework of the Undergraduate Research and Apprentice Program (URAP) at UC Berkeley. The high energy physics group at UC Davis participates in an NSF-sponsored REU program. This program is in its second year and we will actively recruit undergraduate students during the summers. We plan to extend these schemes to the TPC VLSI readout R&D program. This will enable undergraduate students to learn about particle physics and advanced instrumentation while contributing to cutting-edge R&D and studies. We shall encourage women and students from minority-serving institutions to join this program.

Results of Prior Research

The area of R&D we are proposing is quite novel. There has been one earlier attempt, carried out by a collaboration between CERN, Geneva, CEA, Saclay and NIKHEF, Amsterdam. In Spring 2004 they reported to have observed 2D signals from ionizing particles in a small drift chamber equipped with a Micromega foil and readout by means of a MediPix2 chip as direct anode (M. Campbell *et al.*, to appear in Nucl. Instr. Meth. **A**).

LBNL has a long tradition of developing detectors and custom micro-electronics for trackers at both lepton and hadron colliders. This tradition has relied on close collaboration between the Physics and Nuclear Science Divisions and the Engineering Division to blend scientific direction and technical expertise. Not only did the TPC concept originate at LBNL but also the VLSI chip, which we intend to use was developed there. There is very significant expertise both in the construction, commissioning and testing of gaseous detectors, in readout electronics and microelectronics development, which makes such a project particularly well adapted for LBNL. The Department of Physics at UC Berkeley has very tight links to LBNL, but also profits from a mechanical shop providing low charge rates and access to the facilities of the Engineering department in Cory Hall.

The UC Davis group has a long history of R&D in Si pixels starting with the SDC detector at the SSC, followed by the development of generic data-push architecture readout chips and more recently, in the forward pixel group of the CMS Collaboration at the LHC.

Facilities, Equipment and Other Resources

The proposed R&D will be primarily carried out in the newly setup ILC R&D laboratory at the Physics Division of LBNL. The laboratory is presently focused on a Laboratory Directed R&D (LDRD)-funded project on monolithic Si pixel sensors for application at the ILC Vertex Tracker. This laboratory provides basic infrastructure and dedicated space for the TPC R&D and is already equipped with networked computing, gas system and DAQ facilities. The project will have access to the departmental mechanical and electronics shops located on the UC Berkeley campus and to the LBNL shops, as well as technician support through the Physics division. A collaboration agreement with the ATLAS group at LBNL (contact K. Einsweiler) will ensure the availability of a full DAQ chain for the ATLAS pixel chips, several chips and the relevant software and support. This will minimize costs and risks for the electronics and DAQ systems.

At UC Davis, the electronics shop has capabilities of designing, simulating and laying out circuits using state of the art software tools. The test lab contains a full suite of instrumentation for high bandwith analog signal analysis and debugging of multi-channel digital logic. The labs are also equipped with hardware and software for FPGA firmware development, VLSI chip design and probing of bare ASICs. A clean room and an electromagnetically shielded room provide space for testing sensitive components. A 32 node Linux cluster is available for large scale data analysis along with 5 TB of data storage space. Computing will be also supported in part through NERSC, under the resources allocated to the LBNL ILC project (ERCAP request 80938).

FY2005 Project Activities and Deliverables

The first year of the project will be devoted to design and proof of concept. The activity will start with the design and construction of a small test drift chamber equipped with MPGDs. The test chamber will be designed to be adaptable to the tests of various micro-pattern detector designs and configurations. It will also be equipped with standard pad readout for functionality tests. After completion of the construction and testing, studies with the ATLAS VLSI readout chip will start. The UC Davis group will develop and fabricate a prototype board for use with the end-cap of the chamber. This board will house all of the service circuitry for the pixel chips and also provide necessary back-end electronics and data acquisition. VLSI chips will be sent to an external contractor for metalization of the bonding pad and then tested. We envisage performing tests with the test chamber using a laser beam, a ^{55}Fe radioactive source and cosmic rays.

FY2006 Project Activities and Deliverables

We expect to achieve a proof of concept for the readout using the ATLAS VLSI chip and 3D imaging within one year from the start of the project. The second year will then be devoted to the construction of the TPC field cage, definition of the custom chip specs and system design. Lab tests will include studies of charge diffusion with different gases, aging tests and detailed electrostatic simulation of the device which will be performed jointly by the Berkeley and Davis groups. This will make possible to define specs for application of this readout scheme to a large scale device, such as the TPC at one of the ILC detectors. The system design activity will be carried out in collaboration with the Electronics, Software and Instrumentation group in the Engineering division at LBNL (contact P. Denes) that is already a partner in the R&D activity on monolithic Si pixel sensors. It will address issues such as minimization of nearby pad crosstalk, input protective circuitry to eliminate discharge damage and optimisation of dynamic range. Design for the inclusion of the MPGD mesh into a monolithic device will also be carried out, with the aim of achieving a highly integrated device with single electron sensitivity. We expect that significant collaboration with other institutions will be set up at this stage.

FY2007 Project Activities and Deliverables

The third year will be devoted to the engineering design of the TPC end-plates and to finalization of chip design and submission of a first test chip. Engineering tests for the mesh integration will be performed. The test chip will be characterized and tested in the TPC test chamber.

Budget justification:

Lawrence Berkeley National Laboratory

The budget request for FY05 covers the costs for the construction of the test chamber. We intend to profit from our access to the mechanical shop at the Dept. of Physics on the Berkeley campus which offers highly competitive charge rates. Additional items are the post-processing metalization of the chip input pads and the customization of the single chip hybrid and PC board. While we are evaluating the possibility to perform the lithographic metalization in collaboration with the Dept. of Engineering at Berkeley, we cost it at the rate quoted by the MESA Research Institute of the University of Twente in the Netherlands, which successfully processed the MediPix chip for the CERN+CEA+NIKHEF group. The "Other Professionals" cost covers a technician for FY05 and the part of the cost of a part-time micro-electronics designer from LBNL for FY06 and FY07. We expect to receive matching support from the base program at the Physics Division at LBNL, through the ILC project in FY06 and FY07. Equipment costs include the estimated costs for the construction of the test chamber and the high-precision MPGD and VLSI array holder for FY05, the construction of the TPC field cage for FY06 and a fraction of the cost of the test chip submission for FY07. The requested travel funding will cover participation to one topical conference or a dedicated working meeting per year and travel costs to Davis. "Other direct costs" includes a visitor from Europe in FY05 to help with the setup of the Micromega mesh.

Three-year budget, in then-year K$

Lawrence Berkeley National Laboratory

Item	FY2005	FY2006	FY2007	Total
Other Professionals	10	30	30	70
Graduate Students	0	0	0	0
Undergraduate Students	3	3	3	9
Total Salaries and Wages	13	33	33	79
Fringe Benefits	4	11	11	26
Total Salaries, Wages and Fringe Benefits	17	44	44	105
Equipment	20	15	20	55
Travel	5	3	3	11
Materials and Supplies	3	3	3	9
Other direct costs	5	0	0	5
UC Davis subcontract	21.5	49.2	49.6	120.4
Total direct costs	72	114	120	306
Indirect costs	16	25	26	67
Total direct and indirect costs	87	139	146	372

Budget justification:

University of California at Davis

Salary support is requested for a graduate student for the summer of the first year and two academic quarters during years two and three of this project. A total of 400 hours of undergraduate student support (costed $7.25/hour) is requested for each year. Travel support is requested for frequent trips to LBNL. Additional support for travel to one domestic and one international Linear Collider workshops each year is requested for the senior researchers. The supplies budget of $3K/year is for miscellaneous electronics parts, software licences, telephone and printing charges.

Three-year budget, in then-year $

University of California at Davis

Item	FY2005	FY2006	FY2007	Total
Other Professional	0	0	0	0
Graduate Student	6,714	21,821	21,821	50,356
Undergraduate Student	2,900	2,900	2,900	8,700
Total Salaries and Wages	9,614	24,721	24,721	59,056
Fringe Benefits	288	294	300	882
Total Salaries, Wages and Fringe Benefits	9,902	25,015	25,021	59,938
Equipment	0	0	0	0
Total Travel	4,200	5,200	5,400	14,800
Materials and Supplies	3,000	3,000	3,000	9,000
Other Direct Costs (Grad Student Fee Remission)	0	7,346	7,493	14,839
Total Direct Costs	17,102	40,561	40,914	98,577
Indirect Costs	4,447	8,636	8,728	21,811
Total Direct and Indirect Costs	21,549	49,197	49,642	120,388