Project Overview

This proposal presents a request for continued funding for the development of a prototype long-ladder silicon-strip tracking module to be deployed in a test beam in 2006. For the current year, the program was funded from this source at a level of $72,000; we are requesting similar amounts over each of the following two years. This should enable us, in collaboration primarily with LPNHE Paris and Fermilab, to explore the feasibility and advantages of using such an approach to central tracking for a Linear Collider Detector with a testbeam run in 2006. The work described in this proposal, focussed on hardware development, will be complemented by simulation studies undertaken at SCIPP, SLAC, and elsewhere, that will address the feasibility and relative advantage of such an approach for reliable pattern recognition and energy-flow calorimetry. This complementary simulation work, already underway, is not a subject of this proposal.

As will be discussed below, current-year funding has been used to complete the design of a front-end low-noise, long shaping-time analog ASIC, known as the ‘LSTFE’ (Long Shaping-Time Front End) chip. The LSTFE design was submitted to the MOSIS fabrication consortium at the end of 2004, and is just now back in the SCIPP lab and being prepared for testing. Most major components of the LSTFE test setup (LSTFE-specific PC test board, calibration and readout capabilities, and analysis software) have been developed and are now being deployed for testing. We expect to have first results to share by the International Linear Collider Workshop in March.

The focus of the activity over the next two years will be to: 1) Re-optimize the LSTFE in order to take greatest advantage of the recent accelerator technology choice (the first prototype was
geared towards the most challenging scenario, which was the warm accelerator technology); 2) Develop a full readout system, including appropriate back-end ASIC implementations, as well as an FPGA-based readout interface, that will be part of a mutual test-beam effort between LPNHE and SCIPP, most likely to be mounted at the FNAL LC testbeam facility; 3) Contribute to the design and construction of the testbeam prototype hardware; 4) Participate in the test beam run and the analysis of data acquired from the run.

To exploit the tremendous potential of a high-energy electron-positron linear collider (LC), it is necessary to develop a powerful central tracking system. This system needs to determine the momentum of charged particles to unprecedented precision (better than $5 \times 10^{-5}$ in $\delta p_\perp/p_\perp$), avoid the excessive use of material for support and readout, and be able to reconstruct tracks in the notoriously noisy (at least by electron-collider standards) linear collider environment. The work discussed here represents one possible implementation of central tracking for the international ‘Silicon Detector’, which features an all-silicon central tracker, allowing for a relatively compact design that should permit the use of silicon-tungsten electromagnetic calorimetry at reasonable cost. As will be discussed below, the long shaping-time approach promises to minimize the amount of material in the tracker, leading to superior momentum resolution over the full range of track momenta, as well as limiting the degradation of charged and neutral particles before their entrance into the calorimeter, particularly in the forward region. The proponents of this proposal are in close and ongoing contact with the leaders of the silicon detector design study group.

Due to the high precision of microstrip detectors, such a tracker would meet the LC momentum resolution goals. With long ladders, the detector would be burdened by a minimal amount of readout servicing. By turning the power off when not needed, the detector could avoid active, liquid-based cooling. As a result, the tracker would incorporate a minimum of material, and thus maintain its superior momentum resolution at relatively low momentum. As importantly, such a tracker would also impose a minimal amount of material between the tracker and calorimeter, limiting the degradation of the calorimeter response, and the obfuscating effects of conversions and material interactions, particularly in the forward region.

We are proposing the long-ladder solid-state tracker as a specific implementation of the March 2001 baseline SD tracker design of the American Linear Collider Physics Group (ALCPG). In this design, the five-layer central tracker extends between radii of 20 and 125 cm, with a solid-angle coverage of $|\cos \theta| \leq 0.8$, and is immersed in a 5T solenoidal magnetic field. We are also exploring, through simulation, other detector configurations (such as an eight-layer geometry) that may prove more optimal when aspects of pattern recognition are considered.

The keys to achieving the superior tracking performance discussed in this proposal are the use of: (1) long shaping-time electronic readout to reduce voltage-referenced detector noise; and (2) power cycling to eliminate the need for active cooling. We believe it will be possible to exploit these techniques to eliminate everything except the material of the sensors themselves and a minimal amount of support material from the active tracking volume; the detector would be read out at its ends only. In addition, for the inner tracking layers, whose ladders need not be as long as those of the outer layers, the reduced noise may allow the use of thinner sensors. Figure 1 compares the transverse momentum resolution of the baseline L (TPC-based; dashed trajectory) and SD (silicon microstrip tracker with conventional readout; dotted ‘Thick’ trajectory) detectors to that of an idealized short-shaping time detector (‘Thin’ trajectory), for which the only material is that of the sensors themselves. Although not completely realistic, the figure shows that substantial gains in momentum resolution in the
Figure 1: Comparison of the expected momentum resolution at \( \cos \theta = 0 \) for the ‘L’ and ‘SD’ tracking options. The ‘SD’ option is further divided into two scenarios: a ‘Thick’ design with 1.5\( X_0 \) per layer, and a ‘Thin’ design, with 0.3\( X_0 \) per outer layer, and 0.2\( X_0 \) per inner layer.

low-to-intermediate momentum region stand to be made by pursuing the long shaping-time design.

Another major advantage of this design would be its lack of endplate structures and servicing. The separation of \( W \) and \( Z \) bosons via energy-flow calorimetry is a critical component of Linear Collider detection, and production processes tend to concentrate these signals in the forward direction. A long shaping-time microstrip tracker, on the other hand, holds out the promise of minimal material in the forward region: a light support structure, and limited electronics and servicing to read out the relatively few channels at the ends of the long detector ladders. The long shaping-time concept offers the prospect of a tracker that introduces only a small fraction of a radiation length even in the forward region, rather than the large fraction of a radiation length typical for gaseous tracking designs, or the substantial end-region material associated with the readout and cooling of a conventional microstrip tracker (the ATLAS semiconductor tracker has between 30\% and 40\% of a radiation length in the forward region, although admittedly there was less of a motivation to reduce the material burden in that case). This could be a substantial advantage for energy-flow calorimetry, and would eliminate much of the problem associated with conversions and interactions in the detector material.

**Broader Impact**

As an integral component in the drive to develop an optimized design for a Linear Collider detector, this project will contribute to the overall goal of deepening our insight into the fundamental makeup and laws of operation of the natural world. Within this lofty goal, however, lies a much more practical opportunity to train students, from the undergraduate through the postdoctoral level, in a number of broadly applicable technological areas. In addition, as part of the interdisciplinary and well-integrated SCIPP laboratory, this work acts in significant measure to support and further a broad array of scientific efforts.
For example, work done to date in developing our test and readout infrastructure (see below) was funded mutually through, and is currently enjoying application in, both the LSTFE project as well as the Particle Silicon Tracking Microscope (PTSM) project, a collaboration with the Loma Linda medical research center to develop proton-beam based tomography for more effective treatment of human malignancies. Two undergraduates did substantial programming work for control, readout, and data acquisition for the mutual LSTFE/PTSM readout system. Two graduate students gained substantial experience in detector physics through the development of the SCIPP microstrip pulse-development simulation; a third will take over the project and apply it to the upcoming re-optimization of the front-end chip parameters. Two postdocs are involved in the overall development of the test system, including the developing SCIPP expertise in FPGA programming, which will have a broad benefit throughout the lab’s projects in particle physics, experimental astrophysics, radiobiology, and neurophysics. Work supported by this program would continue this contribution to the specialized education of a broad range of students, and to the infrastructure essential to the interdisciplinary program at SCIPP.

Results of Prior Research

In Fiscal Year 2004, this work has been supported by a year of funding through this program (referred to below as ‘current funds’), with an amount of $72,000 received in September, 2004. These funds were made available as a supplement to award DOE-FG02-04ER41286, with a total amount of $1,707,851. In Fiscal Year 2003, this work was supported through a supplement of $50,000 to the same award number, with funds provided through the Advanced detector R&D (ADR) program (referred to below as ‘prior funds’). The total award for that year was $1,472,500. This proposal represents a request for a continuation of the FY 2004 funding, at roughly the same level, for two more years, through FY 2005 and FY 2006.

With prior funding, a pulse simulation algorithm developed by Schumm and graduate students Flacco and Young was used to guide the design of LSTFE ASIC readout parameters and architecture. This led to the selection of a shaping time of $\tau = 3 \mu s$, a two-comparator ‘high-low’ discrimination scheme (for which the high threshold discriminates against noise hits, while the low threshold signal is subsequently used to collect pulse-height information used in constructing an accurate centroid), and a time-over-threshold analog readout. This simulation algorithm is currently being incorporated into the global simulation infrastructure by Young and SLAC physicist Norman Graf.

The parameters and architecture suggested by the pulse simulation studies were incorporated in the LSTFE design, which was implemented in the TSMC 0.25 $\mu$m mixed-signal RF process. Much attention was paid to return-to-baseline and recovery issues associated with rapid power cycling, resulting in a design allowing for a live-time of only 120 $\mu$s per measurement, corresponding to a 1.5% duty cycle for a 120 Hz machine repetition rate, and a corresponding power savings of 98.5%. The design and layout of this chip was completed by engineer Spencer in November 2004, at which point it was submitted to the MOSIS consortium for fabrication. The fabricated ASIC is now in hand at SCIPP, and the process of characterizing its behavior is getting underway. Support for Spencer’s contribution to the design of the LSTFE ASIC was derived from a combination of prior and current funding.

In parallel, much work was completed on the testing infrastructure for the LSTFE project. A PC board that provides power, readout and control traces, and calibration signals to the LSTFE was designed and fabricated, and is now in hand. This PC board, as well as an
expanded view showing the LSTFE prototype ASIC, is shown in Figures 2 and 3. Much progress was also made on the development of an FPGA-based data acquisition system – progress that represents a new capability for the SCIPP laboratory, and one that we expect to lead SCIPP to an expanded role in the development of back-end digital architecture for the LSTFE and other projects. While the contribution of postdocs Nesom and Kroseberg was supported by the base program, approximately $12,000 of current funding was applied to the fabrication of the PC board and the acquisition of electronic control and data acquisition hardware.

Four months into the project (we received the initial $72,000 in Sept 2004), in part due to a prior Advanced Detector R&D grant, we are well along the path towards the production and testing of the LSTFE chip. We are now close to first results with the LSTFE chip, and expect to be able to present them at the International Linear Collider Workshop in late March 2005. Since the period covered by current funding extends into the future, substantial current funds remain to support this work over the next few months. Plans for the use of these funds will be discussed below.

at the quality of the charged and neutral tracks that enter the calorimeter), for which signal-to-noise is a concern.

Facilities, Equipment and Other Resources

The facilities at SCIPP are ideally suited to carry out the proposed work. Over the past two decades, SCIPP has become increasingly expert in the development and application of front-end electronic circuitry, and has amassed the infrastructure necessary to operate effectively in this demanding field. Sophisticated technical equipment, such as an automated wire-bonding facility, micro-probe stations, and semiconductor and network parameter analyzers, essential to carrying out this sort of R&D, have been accumulated through the pooling of funds from diverse R&D projects, as well as through research instrumentation initiatives
(an NSF MRI award in 1997 allowed us to purchase state-of-the-art automated bonding and probe stations that have played a central role in a number of subsequent projects). In addition to our numerous R&D projects, we have recently completed two successful large-scale procurement projects for ATLAS and GLAST. SCIPP currently employs, on a full-time basis, a senior electrical engineer (Spencer, who is a proponent of the proposal), as well as three electrical/electromechanical technicians. The SCIPP facility comprises 5,270 square feet of assignable laboratory space on the second floor of the Natural Sciences II building, which lies at the heart of the cluster of buildings known as ‘Science Hill’ on the UC Santa Cruz main campus.

**Proposal for Future R&D**

At the time of the accelerator technology decision, we decided to proceed with the finalization of the LSTFE design we had at the time, even though it was largely optimized for the beam structure of the warm accelerator technology (the most challenging of the two beam structure scenarios). We felt the extra months of delay we would have incurred in re-optimizing and then redesigning the chip would not have been an effective use of resources; we have enough to learn from the original design about noise performance and power-switching capabilities that we didn’t feel it appropriate to hold up the submission.

With this chip now submitted, and testing beginning, it is time to begin the re-optimization of the LSTFE front end to take greatest advantage of the relaxed beam structure presented by the cold accelerator technology. This reoptimization will begin with simulation studies, making use of the pulse simulation algorithm developed for the original optimization. Re-optimized readout parameters, together with the experience gained from the tests of the existing prototype, will be two of the three essential elements to inform the design of the second prototype. The third element will be the digital and mechanical constraints imposed by the need to incorporate the chip into the mutual test-beam setup that we plan to begin
developing with LPNHE Paris and Fermilab.

In more detail, the relatively relaxed time structure of the cold accelerating technology allows us to entertain the notion of a pulse-by-pulse time stamp for central tracker hits. To good approximation, the time resolution of a discriminated electronic signal is given by

$$\sigma_t = \tau \cdot \frac{1}{\theta - a/\theta^2}$$

where $\tau$ is the preamplifier response (‘shaping’) time and $\theta$ the signal-to-noise ratio. The threshold parameter $a$ is the value of the comparator level (voltage at which the comparator, or discriminator, fires) in units of RMS noise.

For the warm technology, for which pulse-by-pulse timing is not possible for a long shaping-time, low-noise amplifier, the optimal shaping time was found to be $\tau = 3\mu$sec. This leads to a timing resolution of $\sigma_t \simeq 300$ nsec – not quite good enough for a three-sigma identification of individual cold-technology beam pulses, which are separated by 337 nsec. The idea we would like to pursue is to reduce the preamplifier shaping time to improve the timing resolution. This will come at some cost in extra noise, which grows in inverse proportion to the square root of the shaping time. However, we can compromise somewhat on the thickness of the sensors mounted on the longer outer layers of the central tracker, for which signal-to-noise is a concern (note that an additional few hundred microns of silicon will have little effect on the tracking performance of the detector of the quality of the charged and neutral tracks that enter the calorimeter).

The SCIPP pulse development simulation will provide all the information we need to explore operating points that are viable in terms of efficiency and occupancy, as well as to estimate the timing resolution ($\theta$ and $a$ are products of the simulation, while $\tau$ is an input), and thus optimize the shaping time of the next prototype front-end chip. In addition, our prior assumption of 120 Hz operation (warm accelerator technology) pushed the limits of our ability to achieve the necessary power reduction from power cycling necessary to avoid the complication and material burden of active cooling. With the cold technology now selected, which operates at 5 Hz, the permissible switch-on time has been increased by an order of magnitude, allowing us to relax the design in this area, and push a little more aggressively in areas that will contribute to the timing and position resolution (overall noise performance at a given shaping time, immunity to process variation and matching issues, etc.).

We have recently begun to participate in monthly video meetings between Fermilab, SCIPP, and LPNHE, the topic of which is the general application of silicon tracking to a Linear Collider detector. One of the points of focus of these meetings is the demonstration of the long shaping-time concept, and we are beginning to envision a mutual test-beam run to test the complementary LPNHE and SCIPP readout schemes, to provide a common proof-of-principle and to help choose between several different approaches to implementing the long shaping-time front end. This run would likely take place at FNAL in late 2006, and in our monthly meetings we are beginning to discuss the details of how this might play out. Through their extensive involvement in the development of the D0 upgrade silicon tracker, the Fermilab group brings a large degree of expertise in the design and implementation of silicon tracking. In addition, we are exploring the use of sensors from the D0 upgrade project, which have design parameters close to what we are envisioning for the Linear Collider Detector, in the testbeam effort. We will continue to flesh out the details of this collaboration in the coming months, as each participating institution evaluates its area of expertise and capacity for contributing to the project.
As we continue our current work here at SCIPP, much of the resources from the first year’s ($72,000) award remains in hand. While we have been making heavy use of engineer Spencer’s time, we managed to pay for the run of the existing prototype with prior funds. Thus, we have the resources in hand to continue to employ Spencer in the re-optimization of the preamplifier ASIC, even though this was not an anticipated turn of events in our prior proposal.

Thus, the work we envision doing over the duration of the current year’s funding, and then the two years represented in this proposal, is as follows.

In the nearest term, we will place highest priority on testing and gaining experience from the existing prototype. The testing infrastructure is largely in place for this; we will need to fabricate another PC board (to connect the existing Detector Board of Figure 2 to the FPGA-based readout system), and perhaps purchase one or two more minor pieces of laboratory equipment (DAQ card, pulser) depending on the availability of SCIPP laboratory stock. The money for this is in hand from the current year’s funding. The manpower for this will be provided by post-docs Nesom and Kroseberg, supported from our base grant, consulting with Engineer Spencer and technician Wilder. Most important will be to explore the performance of the most challenging aspects of the design: the rapid power switching and recovery, and the noise performance.

Schumm will work with new Ph.D. graduate student Winstrom (who will do his thesis on BaBar) in using the SCIPP pulse development simulation to re-optimize the readout parameters. No support will be required for this. We will then use current-year funds intended for prototype fabrication (but released by our use of prior funding for fabrication) to support Spencer in the design of the re-optimized front-end ASIC.

Year one of proposed funding will be used to finalize the design of and fabricate the re-optimized ASIC, and to provide funds for engineer Spencer to support us in testing the re-designed ASIC, and the implementation of the ASIC in the development of the testbeam prototype (Spencer has extensive experience in the electronics and electromechanics associated with physical tracking systems through his efforts on BaBar, GLAST and ATLAS). We would also bring a graduate student on to help us carry out the test beam effort. This student’s funding would extend into the second year of the proposal, allowing her/him to become engaged with the testbeam effort for an entire year, including the development of components of the testbeam prototype, the running period, and data analysis. This should provide an excellent opportunity for an early graduate student. Second-year funding will also go towards supporting a technician to construct components of the testbeam prototype. We will need to construct at least one more PC board to implement the re-optimized prototype chip in the testbeam prototype. Finally, Spencer will continue to direct the electrical and electromechanical aspects of the testbeam prototype design, and move into the discussion of design of the full tracking system, including optoelectronic (data transmission) issues, which could be critical should thinking continue to favor a triggerless detector.

We expect to augment funding from this initiative with a degree of support from the SCIPP base budget. Postdocs Nesom and Kroseberg, while both heavily involved in BaBar, will work part-time on the LSTFE project. This has already worked quite successfully, with Kroseberg and Nesom having produced a refereed publication from BaBar data in their first year at SCIPP, while also having played a central role in the development of the LSTFE test and FPGA readout infrastructure. We also have base funding to support some amount of travel when it becomes time for the testbeam run.
FY2005 Project Activities and Deliverables

Activity in the first portion of FY2005 will focus on completion of the design and fabrication of the re-optimized LSTFE ASIC. In addition to the re-optimized front end, this ASIC will have an input geometry and data-flow architecture consistent with its use in the joint testbeam prototype. The deliverable will be the fabricated ASIC to the SCIPP lab for testing, with a milestone date of December 1, 2005.

The latter part of Calendar Year (CY) 2005, as well as the first few months of CY2006, will be devoted to characterizing the reoptimized ASIC’s power switching, noise performance, and timing resolution capabilities (the latter of which becomes essential for the reoptimized front-end). We will also explore how far towards the noise floor the second (lower) comparator can be lowered before an unacceptable level of noise is introduced into the centroid-finding algorithm. These results can then be fed back into the pulse development simulation (soon to be part of the global Linear Collider simulation package) to produce a refined projection of the performance of a long shaping-time silicon strip tracker. A deliverable, expected June, 2006, will thus be a re-evaluation of the capabilities of a long shaping-time tracking system for a Linear Collider detector, based on input from lab-bench measurements.

In the latter half of FY2005 (first half of CY2006), we will begin contributing to the design and construction of components for the mutual test-beam prototype, in collaboration with LPNHE and FNAL. We will also develop the LSTFE-specific components of the testbeam prototype (the readout and data acquisition), and contribute to mutual analysis software. Timelines for deliverables for this work will extend into FY2006.

FY2006 Project Activities and Deliverables

In the first few months of FY2006, we will complete the design and construction of the testbeam prototype, including electronics instrumentation and readout. Since the details of this prototype system are just now coming under discussion, it is difficult to specify SCIPP’s full commitment. However, a primary set of deliverables, with a milestone date of October, 2006, will be the full readout, data acquisition, and analysis system necessary to operate and record high-quality data in a two-week testbeam run to be conducted in autumn of 2006, very likely at the FNAL Linear Collider test beam facility. The goal of the testbeam run would be to confirm and refine many aspects of the system performance for which we now rely on the pulse-development simulation, including efficiency and occupancy levels as a function of the track entrance angle, and the point and timing resolutions for minimum-ionizing tracks.

This work would be carried out in large measure by an as-of-yet to be identified graduate student, who would begin working on the project for the last quarter of FY2005, and follow through the first three quarters of FY2006, to the completion of the analysis of the testbeam data. PI Schumm expects to make use of sabbatical release time to see the project through at this point. Thus, a deliverable with a milestone date of the end of FY2006 will be a complete analysis of test beam data, with a clear statement of how that data enhances our understanding of the overall performance of a long shaping-time silicon strip central tracking system.

FY2007 Project Activities and Deliverables

We don’t feel we’re in a position to evaluate our needs for FY2007. We hope that by the end of FY2006 (June 2007), we have in hand a proof of principle of the long shaping-time concept that can fully inform a debate about the design of the Linear Collider Detector(s).
**Budget Justification:** Santa Cruz Institute for Particle Physics

In the description that follows, indirect costs are included in the estimates of expenses. Indirect costs are broken out explicitly in the budget table of the following section.

In the first year, we will complete refinement of the design of the front-end ASIC, and develop a back-end architecture commensurate with testbeam hardware that we expect to develop jointly with LPNHE and FNAL. This will require funds for the fabrication of a final prototype ASIC (about $30,000), as well as an estimated 2-3 months of work from engineer Spencer (we ask for 2.5 months, or about $28,000). We will also need to design at least one PC board to implement the LSTFE ASIC on the prototype detector, and to provide an interface to the FPGA-based readout system (about $4,000; including miscellaneous supplies, this results in a total of about $7,000 for materials and supplies). Finally, as the effort to design and construct the testbeam prototype matures, we will want to bring on a graduate student who will play a lead role in carrying out the testbeam run (about $10,000 for the first of four quarters of support).

In year two, support for the graduate student would extend for three more quarters, through the testbeam run and the data analysis (an additional approximately $28,000). Electrical technician Forest Martinez-McKinney, who is also skilled at mechanical work, would support the final preparation of the testbeam system for about three months (about $19,000). A contingency of about $3,000 ($4,500 including indirect costs) is included for minor laboratory equipment and supplies.

The total request is $75,000 per year for two years, or $150,000 in two years. Although this work will represent a collaboration between SCIPP, LPNHE, and FNAL (and perhaps other institutes that may join later), the funds requested here are to be used solely for the work performed at SCIPP. SCIPP has played a role similar to that played here by LPNHE in expressing support for this mutual effort to European funding agencies (specifically, the DESY PRC). This funding request is intended to allow SCIPP to continue to contribute to the exploration of long shaping-time readout for a Linear Collider silicon central tracker.

**Three-year budget, in then-year K$** Santa Cruz Institute for Particle Physics

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