Project name

Design and Fabrication of a Radiation-Hard 500-MHz Digitizer Using Deep Submicron Technology

Classification (accelerator/detector: subsystem)

Accelerator

Institution(s) and personnel

The Ohio State University, Department of Physics:
K.K. Gan (professor), Richard Kass (professor), Chuck Rush (electrical engineer)

Stanford Linear Accelerator Center:
Steve Smith (staff scientist)

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Project Overview

The Next Linear Collider (NLC) will collide 180-bunch trains of electrons and positrons with bunch spacing of 1.4 ns. The small spot size (σ_y < 3 nm) at the interaction point requires precise control of the emittance, which in turn requires the alignment of individual bunches in the train to within a fraction of a micron. Multi-bunch beam position monitors (BPMs) are to determine the bunch-to-bunch misalignment on each machine pulse. High bandwidth kickers will then be programmed to bring the train into better alignment on the next machine cycle. A multi-bunch BPM system using an 11-bit digitizer with 500 MHz bandwidth and 2 G samples/s is needed to distinguish adjacent bunches. The digitizers are also needed for the low level RF controls in the damping rings and main and injection linacs. Without the digitizers, a redesign of the low level RF technology will be needed. Thousands of channels of digitizers are needed for the NLC. At the present time commercially available digitizers cost $10,000 per channel and are most likely not radiation resistant.

We propose to design a digitizer chip using the deep-submicron technology that has proven to be very radiation hard (up to 60 Mrad). This mitigates the need for costly shielding and long cable runs while providing ready access to the electronics for testing and maintenance. Once a digitizer chip has been successfully developed via several prototype runs, an engineering run at a cost of ~$150,000 will produce all the chips necessary for the NLC. This project will be performed in close collaboration with SLAC.

Description of first year project activities

The digitizer chip is very challenging: large bandwidth (500 MHz), high resolution (11 bits), and fast sampling speed (2 G samples/s). We plan to capitalize on the experience of our engineering staff that, over the last ten years, has designed radiation hard chips for ATLAS, CLEO III, and CMS. Our most recent design of the DORIC and VDC chips for the ATLAS pixel detector uses the IBM deep submicron technology with feature size of 0.25 μm to achieve radiation hardness. We will investigate using the same technology for the design or the newer technology with smaller feature size, 0.13 μm. We will submit a design for fabrication in Multi-Project Wafer (MPW) runs via MOSIS. Due to the complexity of the project, we expect it would take at least two years and three prototype runs before developing a chip that meets the design specifications. We anticipate that we will submit only one MPW run during the first year of this project as a large fraction of the first year time will be spent doing the initial simulation and layout. We believe that the design work is sufficiently complex and must be done by an experienced senior electrical engineer.

We will investigate various possible implementations of the chip. One choice is to develop an analog waveform recording circuit and then do the digitizing more slowly after the pulse has gone by. Another possible implementation is to use multiple digitizers in the chip and route the signal to different digitizers for parallel processing. The various possibilities will be simulated and a design will be chosen for submission for MPW fabrication.

If this proposal is funded, we will go to SLAC to learn more about the system needs for the multi-bunch BPM and low-level RF circuitry. Perhaps some of BPM and RF electronics can be included in the digitizer chip allowing for a more systematic approach to the overall accelerator needs.

Budget

Institution	Item	Cost
OSU	Engineering Time (4 months)	$28,000
OSU	MPW Run (10 mm^2, minimum area allowed)	$15,500
OSU	Test Boards + M&S	$4,000
OSU	Travel	$2,000
OSU	Indirect costs	$22,900
OSU	OSU total	$72,400
SLAC	SLAC total	$0
	Grand total	$72,400