# 4. Vertex Detector

# Vertex Detector Proposals Overview

The Vertex Tracker has to provide the jet flavor identification and accurate track reconstruction that are prerequisites to most if not all of the linear collider physics program. In some detector concepts, the vertex detector takes on an added role of charged particle pattern recognition as well. If the Higgs boson exists and is light, as the data collected so far indicate, its couplings to fermions of different flavour and mass must be accurately measured to test the Higgs mechanism of mass generation. Efficient flavor tagging in multi-jet events and determination of heavy quark charge will be instrumental to study signals of New Physics both through the direct production of new heavy particles, coupled predominantly to $b$ and $t$ quarks, and through precision measurements of electroweak processes at the highest energies. Physics requirements push the vertex tracker specifications to new levels. While much has been learned in two decades of R&D on Si detectors for the LHC experiments, the linear collider requirements motivate new and complementary directions for detector development. The linear collider environment, with its lower event rates and lower radiation, admits Si sensors that are substantially thinner, more precise and more segmented than at the LHC. Technologies which have not been applicable in the high radiation environment of proton colliders are available, as well as sensors based on new concepts. Significant R&D is required to solve the detector problems of the LC environment. CCD vertex detectors have already demonstrated very high resolution and segmentation with moderate multiple scattering. But for the CCD technology to be applicable to the LC improved radiation hardness and a factor of 100-1000 increase in readout speed are required. Technologies successfully developed for the LHC program, such as hybrid pixel sensors, are sufficiently radiation hard and can be read out rapidly. But they now need to be developed into much thinner devices with smaller cell size to improve their tracking resolution capabilities. Finally new technologies, such as CMOS sensors, have emerged as potentially attractive solutions. But they need to be demonstrated on large scales and be tailored to the linear collider application. These developments need to be guided by a continuing program of physics studies and detailed simulations to define the optimal designs and technology choices.

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# (renewal)

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Institution(s)
Fermilab
KEK
Oklahoma
Oregon
Rutherford Lab
SLAC
Yale

Funds awarded  (DOE)
FY04 award: 72,000

New funds requested
FY05 request: 75,000
FY06 request: 150,000
FY07 request: 150,000

# Pixel Vertex Detector R&D for
# Future High Energy Linear e[+] e[-] Colliders

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# 1. Introduction

Studies carried out in the U.S., Europe, and Asia, have demonstrated the power of a pixel vertex detector in physics investigations at a future high energy linear collider. Until recently silicon CCD's (Charged Coupled Devices)[1] seemed like the detector elements of choice for vertex detectors for future Linear e[+] e[-] Colliders. Last year, recognizing the potential of a Monolithic CMOS detector, we initiated an R&D effort to develop such a device. With the recent Technology Decision choosing a TESLA-like superconducting technology for the future ILC (International Linear Collider), the motivation for such a detector technology is even more compelling. The time structure of this cold technology is such that it necessitates an extremely fast readout of the vertex detector elements and thus CCD's as we know them will not be useful. There are discussions of inventing new CCD architectures[2] but these seem rather far ahead of the current state of the art. For these reasons there is an increased importance on the development of Monolithic CMOS pixel detectors that allow extremely fast non sequential readout of only those pixels that have hits in them. This feature significantly decreases the readout time required. Another important feature of our present conceptual design for these CMOS detectors is the possibility of putting a time stamp on each hit with sufficient precision to assign each hit to a particular bunch crossing. This significantly reduces the effective occupancy in that in the reconstruction of any particular event of interest we only need to consider those hits in the vertex detectors that come from the same bunch crossing.

# 2. Objectives of the Proposed Project

We are proposing here the continuation of an R&D program on ILC Vertex Detectors that has been approved and funded this past year. The detailed emphasis of this program has changed somewhat since the technical decision for the cold machine.

### 2.1 Continuation of the Development of the Monolithic CMOS Pixel Detectors

During the past year, in collaboration with SARNOFF, we developed a conceptual design for a CMOS device that we feel will work well for the ILC vertex detector, and that

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[1]K. Abe, et. Al., "Design and Performance of the SLD Vertex Detector, a 307 Mpixel Tracking System," Nucl. Instrum. Meth. A400, 287 (1997)

[2]C. S. J. Damerell, LCWS 2004, Paris, April, 2004, http://hepww.rl.ac.uk/lcfi/public/lcws-damerell.ppt; Y. Sugimoto, 7th ACFA Linear Collider Workshop, Taipei, Nov. 10, 2004, http://hep1.phys.ntu.edu.tw/ACFA7/slides/B-4 Sugimoto.ppt

SARNOFF believes they can build. This coming year we plan to take this design to the detailed engineering design stage and have SARNOFF fabricate the first prototype devices (actual prototypes may have to be delayed another year due to lack of sufficient funding).

## 2.2 Radiation Hardness Testing of Both CCD and the New CMOS Device Prototypes

We plan to complete the radiation testing of CCD's from the SLD vertex detector and start testing the first prototypes of the new CMOS devices. We have a test set up at SLAC with electron beams, and have built an instrumented a beamline at the WNSL Heavy ion accelerator at Yale for radiation testing of imaging devices with proton, neutron, α, and heavy ion beams in the 10 to 40 MeV/nucleon range.

**2.3** We plan to continue a low level of effort on detailed engineering design to minimize the thicknesses of both the detector chips and the support structure of the ILC vertex detector.

# 3. Progress in the Past Year

The overall vertex detector design we are working towards is shown in Figure 1, and the numbers and sizes of the 120 detector elements (chips) are summarized in Table 1.

The detailed time structure of the ILC is still to be settled on in the future. For the purposes of our present design we are using the time structure of the TESLA design. We assume that the ILC design will have similar features. This design has 2820 bunches in a bunch train, with 5 bunch trains per second. The separation between bunches in 337 nanosec, which makes each bunch train about 1 millisec long, with about 200 millisec between bunch trains.

Extensive background calculations indicate that the total hit rate in the vertex detector per layer will be:

Background rate = 0.03 hits/mm$^2$/bunch crossing

## 3.1 Progress on Monolithic CMOS Pixel Detector Design

During the past year, in collaboration with SARNOFF, Inc. (RCA's Silicon Fabrication House) with whom we had an R&D contract, we developed a draft conceptual design for a device (chip) that we believe will work well for the ILC Vertex Detector application and that SARNOFF believes they can make. We will discuss here a typical 22 mm x 125 mm chip to be fabricated by SARNOFF's CMOS process. Each chip would consist of two particle detection layers, which we call Big pixels (Macro Pixel Array) and Small pixels (Micro Pixel Array) (Big pixels ~ 50μ x 50μ, Small pixels ~ 5μ x 5μ) each layer covering the full area of the chip (i.e. ~ 100 Small pixels under each Big pixel). The Big pixels will detect a hit and get the time of the hit (to a precision of better than 1/3 microsec or one bunch crossing time). There will be enough logic circuitry in each pixel that using the location of the Big pixel hit we look for hits in the Small pixels to determine the precise x and y location of the hit and get a 3 bit grey scale of the charge accumulated in each Small pixel. Even a single particle crossing will deposit charge in several Small pixels due to charge spreading beyond a pixel. The 3 bit grey scale is to allow the determination (later in the analysis) of the coordinates of the centroid of the particle to better than a pixel size.

The time information for each hit in the Big pixels is stored under the area of the Big pixels with room for up to 4 hits. At 12 bits + 1 parity bit this requires 52 bits under each Big pixel which is quite manageable as shown in Figure 2. The Big pixels are reset after the time is stored to get ready for the next beam crossing. The Small pixel array stores the analog signal charges locally for the ~ 1 millisec duration of the entire bunch train.

Due to concerns about excessive Electromagnetic Interference during the bunch train, we do not plan to read out the device until after the bunch train when we have a leisurely 200 millisec to read out not all pixels as in a CCD but only the pixels that were hit.

To get some estimates of hit rates and occupancies, we use the estimate of 0.03 hits/mm$^2$/bunch. We then expect an occupancy of ~ $10^{-6}$ per Small pixel and ~ $10^{-4}$ per Big pixel per bunch crossing. Integrating over 2820 bunches in a train we expect about 3 x $10^{-3}$ hits per Small pixel and ~ 0.3 hits per Big pixel in a bunch train. Thus we expect to only rarely exceed the storage capacity of 4 hits in each Big pixel (if need be the 4 hit limit can be increased). The total number of hits per 22 mm x 125 mm device (chip) (with 1.1 x $10^8$ Small pixels) is expected to be ~ 3 x $10^5$ hits/chip. At a read out rate of 25 MHz these hits can easily be read out in well under the 200 millisec gap between bunch trains. The occupancy in the Small pixels, integrating over a bunch train, is expected to be of the order of one percent. This appears much too high to allow efficient pattern recognition. The crucial element of our design is the availability of the time information (i.e., bunch crossing number) with each hit. If we trigger on an event that we are interested in from another part of the detector (tracker or calorimeter) with a time, i.e., the bunch crossing number known, we need to look only at those vertex detector hits which are consistent in time with the event of interest and the occupancy drops to below $10^{-5}$ per Small pixel which is wonderful (SLD worked well with an occupancy of ~ $10^{-3}$ per pixel in the Vertex Detector).

A first design of the architecture of the Big (Macro) and Small (Micro) Pixel Arrays by SARNOFF is shown in Figures 2 and 3.

## 3.2 Progress on Radiation Damage Testing

During the past few years, we have carried out an active investigation into the effects of radiation damage in the CCDs used in the SLD vertex detector. The principal results of these studies are:

Neutron Damage Studies
  Several exposures to neutrons yielded studies of damage, annealing, and charge trapping times. The technique of significantly reducing the effects of radiation damage by injecting sacrificial charge was developed. (references below)

Electron Damage Studies
  NLCTA (Next Linear Collider Test Accelerator) exposures established the difference between electron and neutron effects, and demonstrated that the damage in VXD3 was electron induced. Our method of injecting sacrificial charge to significantly reduce the effect of radiation damage was demonstrated. (references below)

The expected radiation dose at the SLC was less than 1 krad for the lifetime of the SLD vertex detector and the CCDs were tested to operate at a dose of 10 krads. The detailed background calculations for the next generation $e^+$ $e^-$ colliders indicate an upper limit of

100 krads/10 years, a factor of 100 to 1000 higher than at the SLC. The neutron backgrounds are estimated to be ~$10^9$ - $10^{10}$ neutrons/cm$^2$/year, larger than at the SLC by a similar factor. We believe that this increase in radiation tolerance can be achieved by various strategies. Reducing the thickness of the surface silicon dioxide layer will reduce the surface damage from ionizing radiation, and reducing the well size in the pixels will reduce the amount of bulk damage. Furthermore, the use of the sacrificial charge technique will reduce the effect of bulk damage on the charge transfer efficiency. To test the success of these strategies would require the design of a new CCD, the fabrication of these devices by commercial silicon fabrication houses, and radiation testing the resulting CCD. This will not pursued now, in favor of the CMOS detector development.

### 3.2.1 Neutron Damage Studies

Our progress on studying CCD radiation damage has been reported in a number of talks and papers.

J.E. Brau and N. Sinev, "Operation of a CCD particle detector in the presence of bulk neutron damage," IEEE Trans. Nucl. Sci. 47, 1898 (2000).

C.T. Potter, J.E. Brau, and N.B. Sinev, "A {CCD} vertex detector for measuring Higgs boson branching ratios at a linear collider," Nucl. Instrum. Meth. A511, 225 (2003).

J.E. Brau, O.B. Igonkina, C.T. Potter, and N.B. Sinev, "Investigation of radiation damage in the {SLD} {CCD} vertex detector," IEEE Trans. Nucl. Sci. 51, 1742, (2004).

J.E. Brau, O.B. Igonkina, C.T. Potter, and N.B. Sinev, "Investigation of radiation damage in neutron irradiated CCD," to be published in IEEE Trans. Nucl. Sci. (2005).


Our neutron damage studies of several years ago play a key role in our current analysis of damage to VXD3 (below) but are not reported here. However, recent detailed study of the effects in the CCD exposed to neutron irradiation 5 years ago, revealed new facts about the nature of radiation damage. First, we discovered that in the 5 years the CCDs sat at room temperature, no significant annealing of the damage was observed. The decrease in the number of charge traps which had been created by neutron irradiation was less than 5%. Second, we measured the dependence of the degree of charge trapping as a function of time. The trapping time expected, based on prior theory, was in the range of nanoseconds. However, we observed tens of milliseconds are required for complete trapping. We think there is a theoretical explanation, but this was overlooked in the prior theory. The effect has implication for the CCD vertex detector since it predicts less sensitivity to radiation damage effects for CCDs operating at higher speed.


### 3.2.2 Electron Damage Studies

In 2003, we exposed the spare VXD3 ladders to the NLCTA electron beam to measure the effects of radiation damage from electrons. We conducted two similar exposures

of about $5 \times 10^{11}$ electrons/cm$^2$ to two different ladders. The electron energy was 60 MeV. The charge transfer inefficiency through the entire CCD (2000 rows) caused by radiation damage from these electrons was about 30% for one ladder, and close to 90% for the other. This difference is not understood. It may result from different doses, although the experiment was designed to deliver the same dose in both exposures. While all beam parameters were very similar in both exposures, the dose monitor was only active during the second exposure. Another explanation could be different amounts of oxygen in the two detectors. We need more studies to understand this result. The important observation from these studies is that the number of charge traps per pixel created by electron irradiation is significantly different from that of the neutron created charge traps. This has allowed us to measure the relative fractions of neutron induced and electron induced radiation damage in VXD3.

### 3.2.3 VXD3 Radiation Damage Studies

We removed the inactive vertex detector VXD3 from SLD and made detailed measurements of the level and character of the radiation damage from three years of SLD data taking. In addition to normal running, at least once, early in the run, undamped beams were brought through the detector, exposing the CCDs to unusually large levels of radiation. The inner South CCDs were particularly affected as they face the beampipe. The distribution of number of charge traps/pixel indicates that damages were caused by light particles - electrons or photons. The level of damage corresponds to exposure to about $10^{11}$ - $10^{12}$ electrons/cm$^2$ (10 - 100 kRad) if the energy of electrons was similar to NLCTA electrons (60 MeV). If the electron was of higher energy, the estimate of the level of exposure level would be reduced.

## 4. Plans for the Coming Year

### 4.1 Monolithic CMOS Pixel Detector Development

As described above, we believe that we have a conceptual design for these detectors that will work for the Vertex Detector for a superconducting ILC, with even a considerable margin of safety. The next step we believe is to start detailed design of these devices via a contract with SARNOFF that will lead to the fabrication of some small prototypes.

There are many issues and uncertainties that will have to be addressed in the detailed design. Some of these issues apparent at this time are:

- SARNOFF feel they can build devices with pixels as small as 5μ x 5μ, have large area chips, 25 MHz read rate, and sufficient logic under each pixel to do what it needs to do in this conceptual design. Can they achieve all of these features simultaneously on one chip?
- How thin can these devices be thinned below the standard 500μ thickness?
- Radiation hardness
- Power consumption
- Will the Electromagnetic Interference during a bunch train affect adversely the functioning of the device at the pixel level?

We believe that the funding that will be available this coming year will not be sufficient to carry out both the detailed design by SARNOFF and the fabrication of the first prototypes. We foresee two options. The first is to find Japanese or European collaborators to put in some funds to allow SARNOFF to proceed with prototypes this coming year. The second option is to delay the fabrication of the first prototypes after the following year.

## 4.2 Beam induced EMI tests

EMI effects disrupted the planned operation of the SLD vertex detector VXD3, requiring a delayed readout of the CCDs. The origin of these effects was never completely understood, since operations were possible. If such a problem recurred at the ILC, it would not be possible to solve it so easily. Therefore, for the sake of the ILC, it is critical to understand the origin of such effects, and to develop procedures for ameliorating them.

Working in collaboration with groups from Rutherford-Appelton Lab and KEK, we plan to study this problem.

## 4.3 Radiation Damage Testing

In this coming year we plan to complete the radiation testing of the SLD vertex detector CCD's. While much has been learned in the tests to date, there remain unexplained effects, such as the long trapping times, which must be resolved. Such tests might involve electron beams at SLAC and possibly proton beams at Yale. When the first CMOS prototypes from SARNOFF are available, we plan to do radiation testing on those both with electron and proton/neutron beams. This activity will require engineering and technician support for fixturing, vacuum, electronics, etc.

# 5. Relationship to Linear Collider Detector Concept Studies

Our vertex detector design effort is in the context of the SiD detector concept. The design that we are working on, illustrated in Figure 1 and Table 1, fits well within that context and has the parameters appropriate to that detector. However, the other detector concepts, the LDC and GLD designs, also require vertex detectors and our R&D is also exactly relevant to those designs. We thus believe that the R&D we are proposing is important for all of the detector concepts under discussion at this time.

# 6. Relationship to Other CCD Vertex Detector R&D Programs

6.1 This research is coordinated with M Breidenbach, SLAC; A. Miyamoto, Y. Sugimoto, KEK; P. Skubic, U. of Oklahoma; R. Yarema, W. Wester, FNAL; C. Damerell and the LCFI, Rutherford Lab.

6.2 The LCFI Collaboration, in Europe led by Chris Damerell of Rutherford Labs, is developing a CCD vertex detector for the TESLA Detector. We maintain a close relationship with the work of the European group and are coordinating our activities with them to complement, rather than duplicate, their R&D effort.

In the course of the design and successful fabrication of the Yale QUEST CCDs, we have made a number of contacts and worked with several silicon fabricators. We have built on this base of experience and have this year made a subcontract with the SARNOFF Corporation, who is quite experienced in the design and fabrication of CMOS pixel imaging devices, and have developed a conceptual design for our CMOS pixel detectors. We plan to exploit this connection in the future to move on to detailed design and have the fabrication of prototype devices by SARNOFF.

6.3 The Japanese CCD Vertex Detector Collaboration, led by Y. Sugimoto and A. Miyamoto of KEK, is also working on the issues confronting a CCD vertex detector for the linear collider. We are in direct communication with this group, and coordinating our R&D effort, and plan now to write a proposal for the Japan-US Program to develop a vertex detector prototype.

6.4 We have begun work on the readout electronics for linear collider vertex detectors in collaboration with SLAC (M. Breidenbach and G. Haller). There are other groups proposing to work on the fast readout electronics required for these detectors, and we plan to coordinate our efforts closely with these groups so that together we develop a coherent detector with pixel imaging detectors and the electronics appropriate to read them out.

# 7. Work Plan and Deliverables

We are proposing here a three-year R&D program to address the issues discussed above. We foresee the following activities

## 7.1 Work Plan Year 1

- Continue study and design of CMOS detectors for ILC
- Simulation studies of the effects of detector thickness on the physics, and coordination with other groups doing simulations
- Continue the study of effects of radiation damage
- Mechanical Engineering study of support scheme

## 7.2 Work Plan for Year 2

- Complete detailed design for CMOS detectors
- Buy masks for fabrication
- Place order and start fabrication of prototypes
- Continue the study of effects of radiation damage
- Continue support structure engineering design
- Begin ASIC development for readout

  (progress on year 2 work plan will be contingent upon successful supplemental funding to pay for all engineering and masks)

### 7.3 Work Plan for Year 3

- Complete prototype detector fabrication
- Complete prototype ASIC fabrication
- Test performance of prototype detectors
- Radiation test of prototype detectors
- Complete preliminary support structure design

  (progress on year 3 work plan will be contingent upon successful supplemental funding in years 2 and 3 to pay for all engineering and fabrication)

### 7.4 Deliverables after the 3 Year R&D Program

- First prototype devices (contingent on supplemental funding)
- Performance and radiation tests of prototype devices
- Preliminary support structure design

# 8. Budget Estimates

| | Request in Units of $1000 | | |
|---|---|---|---|
| Item | Year 1 | Year 2 | Year 3 |
| Engineering, Technician, Shop Support and Supplies | | | |
| At Oregon | 13 | 25 | 25 |
| At Yale | 12 | 25 | 25 |
| Subcontracts | | | |
| CMOS Design | 50 | 25 | 0 |
| Masks | 0 | 25 | 0 |
| CMOS Fabrication | 0 | 50 | 100 |
| Yearly Totals | 75 | 150 | 150 |

# 9. Broader Impact

This research project contributes to society in many ways, including but not limited to:

- development of new devices for applications in other fields
- opportunities for students and young researchers to learn state-of-the-art techniques
- advances in the understand of the fundamental nature of the universe around us.
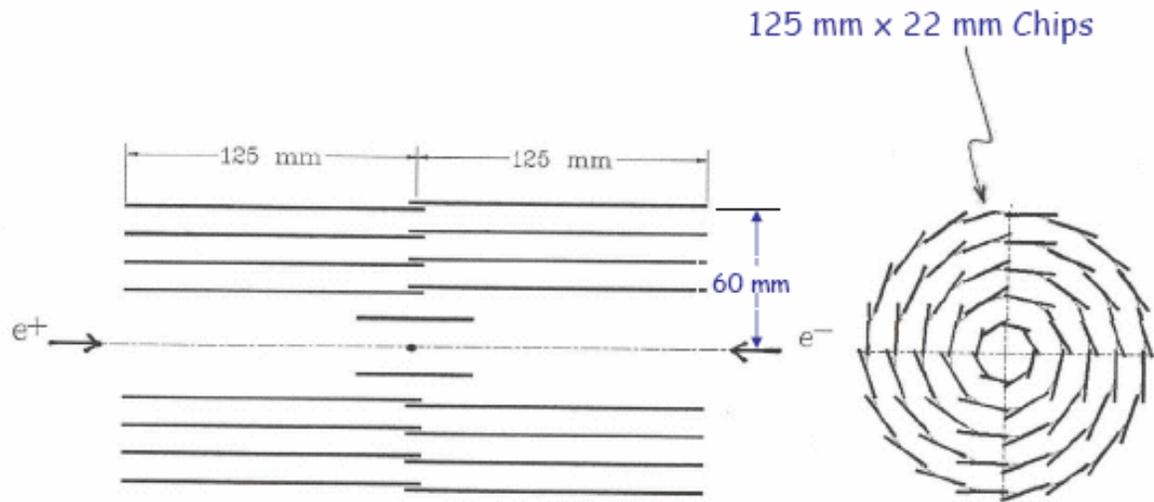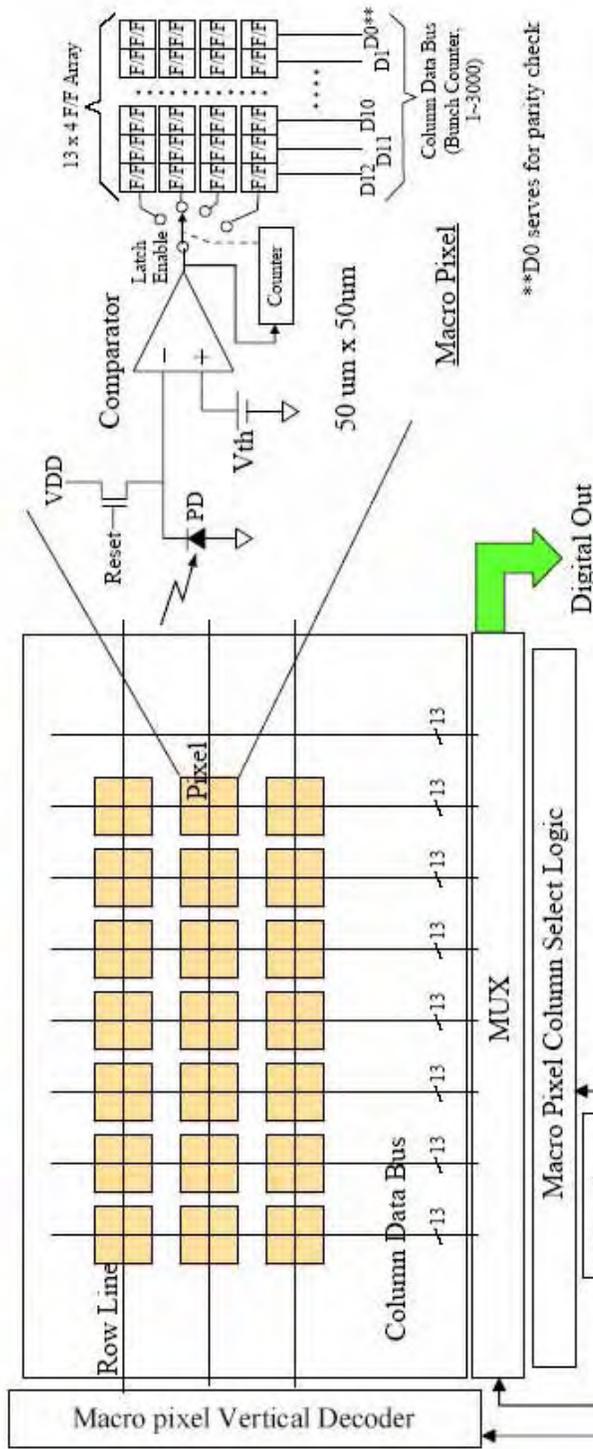
## Vertex Detector Design

Figure 1

## With Monolithic CMOS Pixel Detectors

| Layer | Radius | Total Length | No of Chips | Chip Size |
|-------|--------|--------------|-------------|-----------|
|       | Cm     | Cm           |             | Cm        |
| 1     | 1.2    | 5.0          | 8x1         | 5.0x1.2   |
| 2     | 2.4    | 25.0         | 8x2         | 12.5x2.2  |
| 3     | 3.6    | 25.0         | 12x2        | 12.5x2.2  |
| 4     | 4.8    | 25.0         | 16x2        | 12.5x2.2  |
| 5     | 6.0    | 25.0         | 20x2        | 12.5x2.2  |

Table 1

# Macro Pixel Array Array Architecture



- As a local digital memory to store the time stamp, F/F's are used. To express 3000 bunches, 12 bits are needed and 13th bit is for checking the parity. Since average multiple impact probability per pixel is assumed to be 4, 13 (H) x 4 (V) F/F's are needed in this architecture.
- When a particle impacts, a pixel's signal rises above the threshold level and comparator out switches from '1' to '0', enabling the F/F's to latch the time stamp data supplied by the global bunch counter. When the data is latched, the pixel is reset.
- If next particle impacts the same location, comparator out enables next set of F/F's to preserve the previous time stamp data. This is implemented using a counter which increments the row address of the F/F array.
- Time stamp information is read out in the random access mode from the pixels of interest which stored nonzero time stamp data.
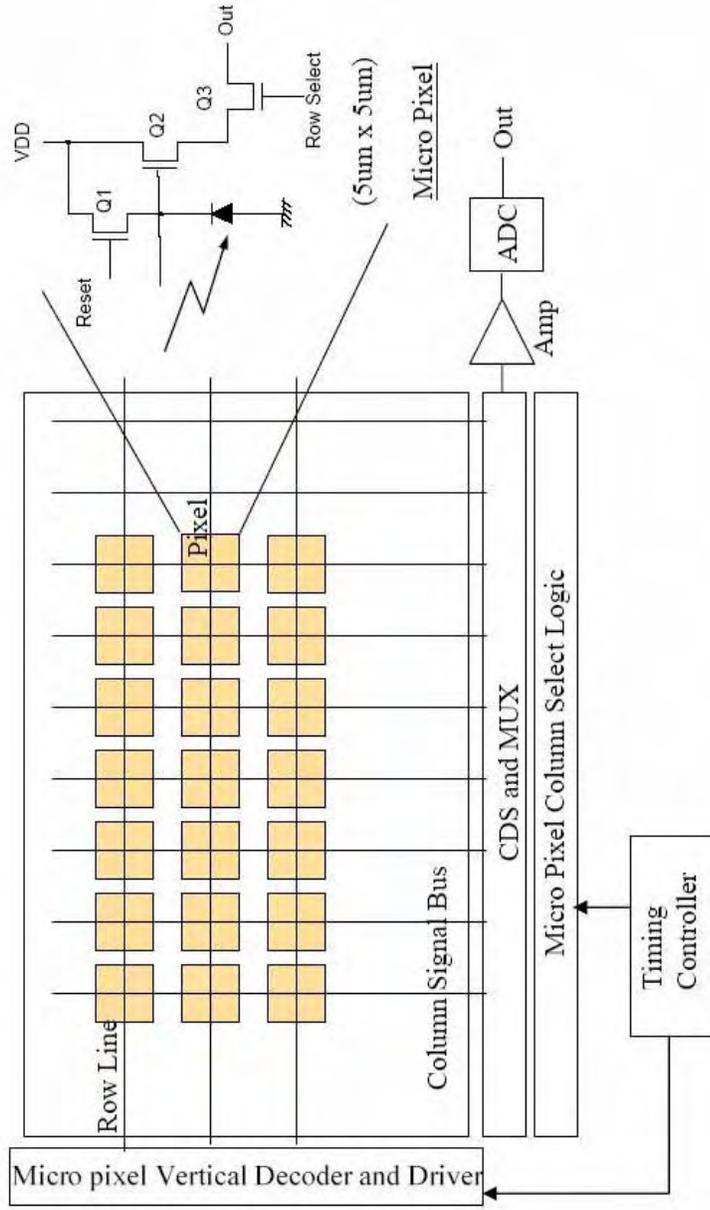
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Figure 2

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# Micro Pixel Array Architecture



Figure 3
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